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Memristors for neuromorphic computing systems: basic parameters and methods of their optimization

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Contents

Abstract. In recent years, the scientific community has maintained substantial interest in neuromorphic computing systems based on memristive devices owing to their unique advantages. Although there is a wide variety of memristors, a device with optimal parameters for neuromorphic computing has not been developed yet. This article presents comprehensive overview of the principal types and parameters of memristive devices. Memristors operating through valence change, electrochemical metallization, phase-change, ferroelectric tunneling, and spin-tunneling effects are considered. The key characteristics, benefits and limitations of each memristor type are analyzed. The main approaches to enhancing parameters of memristors are presented, including optimization of composition and structure of memristive devices, circuit architecture and algorithmic solutions.

Keywords: memristors, mechanisms of operation, type of memristors, characteristic optimization

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1. Introduction

Neuromorphic computing systems (NCS) are systems that mimic the structure and functions of biological neural networks (e.g., the human brain) to perform intelligent computations [1–5]. Unlike traditional computers, NCSs have an architecture that is more like biological systems and can be implemented at the software, hardware, and hybrid levels. NCSs aim to replicate key aspects of biological neural networks, such as parallel and combined information processing and storage, energy efficiency, adaptability and learning. The main elements of NCSs are artificial neurons and synapses. Neurons process input signals and generate output pulses (spikes). Synapses regulate the strength of connections between neurons (synaptic weights) and, accordingly, the amplitude of transmitted signals. Changing synaptic weights allows the network to learn and adapt to the spatiotemporal structure of input data.

The basis for hardware implementation of digital NCS, as for traditional electronic computing systems, are silicon metal–oxide–semiconductor complementary (CMOS) technologies [6–15]. Based on these technologies, specialized processors are being developed to support neural networks, such as tensor and fully digital neuromorphic processors (Google TPU, Altai, Akida, Intel Loihi 2, IBM Northpole). However, despite the many advantages, CMOS processing systems have a number of significant drawbacks for use in NCS. These include delays in the transmission of data due to the need to move it between the CPU's arithmetic-logical unit and a separate memory module (both internal and external), which markedly limits performance and increases thermal energy consumption [16–19]. Also, it is noteworthy that the CMOS chip consumes high amounts of energy, which is associated with leakage even in a power-off state and, consequently, significant heat emission during operation and standby [3 , 8, 20].

Promising elements for the implementation of artificial synapses in NCS are memristors (resistors with memory effect) [16, 21, 22]. The latter are able to change their

resistance depending on the applied voltage and the charge flowing through them [23, 24], which makes them highly effective in simulating synaptic plasticity — a key training mechanism in biological neural networks [25–28]. At the same time, memristors can take many intermediate values of resistance [29, 30], which makes it possible to precisely set synaptic weights (almost in analog mode) and provides a training possibility. In addition, the state of memristor with a certain resistance value can be maintained for a long time without any external stimulus, imitating the long-term memory of a biological synapse [31]. The memristors are capable of operating at low voltages, have a small area and therefore little parasitic capacitance, and can switch between resistive states in nanoseconds, thereby ensuring energy efficiency, high data density and high-speed hardware adjustment of synaptic weights [32–35].

Initially the concept of memristor was introduced by Leon Chua in the early 1970s [36, 37]. He analyzed the relationships linking variables in electrical circuits (current, voltage, charge and magnetic flux) through the characteristics of three existing fundamental bipolar elements (resistance, inductance and capacitance). As a result, Leon Chua concluded that for reasons of complete symmetry there must be a fourth fundamental element of the circuit which would link an electric charge q and a magnetic flux Φ (Fig. 1). This element is called a 'memristor.' The proposed concept was not used for almost 40 years until an article [38] was published reporting the experimental discovery of the missing memristor.

It should be noted that many scientists express doubts about the conformity of currently actively studied memristors and memristors, whose existence was predicted by L. Chua [24, 39–41]. It is justified primarily by the fact that the operation of memristors is not linked to the magnetic flux described in L. Chua's pioneering work. Moreover, a careful examination of this question using Maxwell's equations shows that the existence of a new fundamental element linking magnetic flux and charge seems impossible. However, such a discrepancy does not limit the prospects of using modern-understanding memristors in various practical applications.

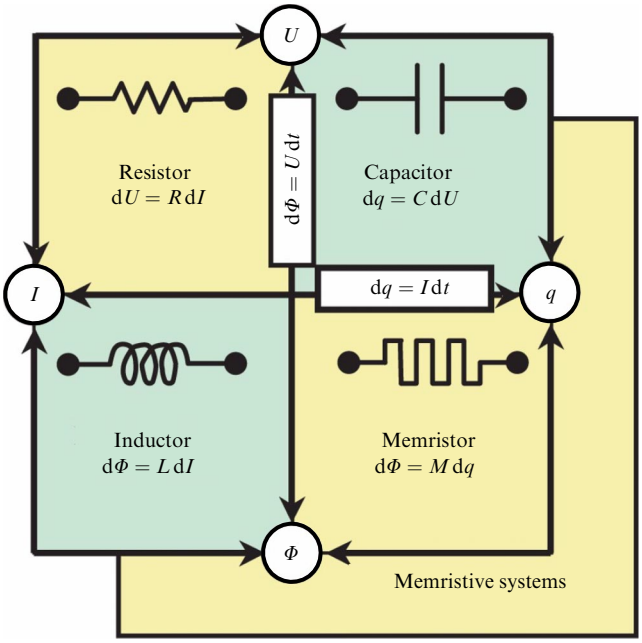

Figure 1. Four fundamental bipolar circuit elements linking current, voltage, charge and magnetic flux according to Leon Chua's theory [38].

Although memristors have enormous potential for applications in NCS, their widespread adoption is hindered by a number of technical challenges. First of all there is the significant parameter variation of memristors (e.g., resistance value variation) due to the nature of resistive switching and insufficiently mature manufacturing processes [33, 42–44]. This complicates their use in large arrays. Furthermore, after a sufficiently large number of switching cycles, memristor parameters may degrade, limiting their endurance and reliability [45, 46]. Additionally, the resistances of memristors are subject to random fluctuations (noise) during storage or readout, which reduces computational accuracy and necessitates the development of complex error correction algorithms [47]. However, in some cases, noise can play a constructive role, for example, in cryptography, random sequence generation, memory trace retention, and other applications [48–51].

To address the aforementioned problems, various approaches and methods are employed. First, the composition and structure of the active switching layers are optimized, typically through doping, controlled defect engineering, or the incorporation of nanoparticles. Optimization of the active layers can also be achieved by utilizing multilayer functional structures, creating a stoichiometric gradient, forming an oxygen vacancy reservoir, adding a heat accumulation layer, or by selecting special alloys for the electrodes [52–60]. A promising direction is also the use of two-dimensional materials (graphene, MoS_2, etc.) as the active-layer [61, 62]. Second, various circuitry and algorithmic solutions are being developed, such as improving the architecture and addressing of memristive arrays and/or their switching methods [33, 63]. Research areas related to the study of photonic [64] and quantum memristors [65–68] are also actively evolving.

In this work, an overview of various types of memristors and their operating principles is provided in order to analyze their advantages and disadvantages. Data on the main parameters and characteristics of various types of memristors are presented; methods for improving their functional properties, which are useful in key applications of memristive elements as synaptic weights in NCS, are described.

2. Memristors and mechanisms of their operation

A memristor is a nonlinear electronic element capable of changing its resistance depending on the applied voltage and the charge that has passed through it, and retaining this state after power is removed [38]. A memristor typically consists of a thin-film structure with two electrodes. To date, a fairly large number of different memristive structures have been investigated, and their diversity can be classified in various ways: by the volatility of their switching (volatile and nonvolatile), by polarity (unipolar and bipolar), and by the resistive switching (RS) mechanism, which is perhaps the most interesting classification from the perspective of the physical principles underlying their operation. Several main RS mechanisms used in NCS are distinguished: valence change (movement of charged vacancies of an oxidizing element (oxygen, nitrogen, etc.)), electrochemical metallization (movement of metal cations), phase transitions, electrical polarization, and tunnel magnetoresistance [69–72].

Switching due to valence change, which occurs through local hops of film anions (oxygen ions) between vacant lattice sites under an electric field — equivalent to the motion of vacancies of that element in the opposite direction — is one of the main mechanisms in metal oxides (e.g., TiO_2, HfO_2, Ta_2O_5, etc.). Under an external electric field, negatively charged oxygen ions (anions) can migrate from the crystal lattice toward the positively biased electrode of the structure, leaving behind positively charged defects (oxygen vacancies) that act as doping impurities. Consequently, in the region where oxygen vacancies appear, the charge carrier concentration increases, and thus the conductivity increases. As a result, a thin conductive filament forms from the generated defects and short-circuits the electrodes of the structure and switches the memristor from the high-resistance state R_{off} to the low-resistance state R_{on}. When the polarity of the external voltage is reversed, oxygen ions return, oxidizing the conductive paths, which causes the structure to switch back to the high-resistance state. This mechanism is based on redox reactions that change the valence of metal cations in the oxide; therefore, it is often called the valence change mechanism (VCM) [73].

Despite the fact that the processes described above occur on atomic scales, high-resolution transmission electron microscopy (TEM) has made it possible to observe the growth of an oxygen-deficient filament and confirm the proposed switching mechanism [74, 75]. Figure 2 shows a series of TEM images demonstrating the formation of a conductive filament in a ZnO film as the applied voltage increases [75]. Also, beneath each TEM image, the corresponding portion of the current-voltage ($I-V$) characteristic is shown. The figure clearly confirms that switching from the high-resistance state to the low-resistance state occurs through the formation of a conductive filament.

At the same time, RS in VCM memristors can differ. Figure 3 shows examples of $I-V$ curves with different RS behaviors. As can be seen from Fig. 3a, switching from the high-resistance state to the low-resistance state and returning back occur at different polarities of the applied bias. This operating mode of a memristor is called bipolar. Moreover, when the voltage is removed, the resistance of the structure does not change (for example, after switching from R_{off} to R_{on} the resistance remains in the R_{on} state after power-off). This mode is called nonvolatile. The nonvolatile mode is necessary for implementing synaptic connections in NCS [76]. Figure 3b shows another case: the structure switches from R_{on} to R_{off} and back to R_{on} without changing the voltage polarity. This RS mode is called unipolar and in this particular case is volatile, since the return from the low-resistance state (LRS) to the high-resistance state (HRS) always occurs when the voltage drops below a certain threshold value $V_{TH2} < V_{TH1}$ of the same (but arbitrarily chosen) polarity. This mode can be used to implement selectors for passive crossbar arrays [77] or to implement a dynamic layer of a reservoir computing system (RCS) [78]. It is worth noting that for some structures, coexistence of volatile and nonvolatile modes is possible by controlling the maximum allowable current through the structure (compliance current) and/or the external temperature [79–81]. For certain memristor active materials, e.g., NiO, unipolar RS may be observed, where the RESET operation is performed with a pulse of the same polarity as that in the SET mode [82–84]. In this case, switching from the low-resistance state to the high-resistance state and back requires different compliance currents (so-called threshold switching). The $I-V$ curve of such a memristor is shown in Fig. 3c. In unipolar memristors, Joule heating plays a key role in the formation/rupture of the conductive filament.

It should also be noted that there are memristors in which resistive switching is not associated with filament formation but occurs over the entire area due to a change in the Schottky barrier at the interface between the electrode and the active layer or a change in the tunneling probability through the active layer [86]. In the case of organic memristors with an electrolyte gate, resistive switching occurs via an electrochemical reaction, also throughout the volume of the active film [87, 88]. This type of resistive switching is sometimes called interfacial (as opposed to filamentary).

The electrochemical metallization (ECM) mechanism is based on the transport of metal cations and redox reactions in simple planar or sandwich metal–dielectric–metal (MDM) structures [89–91]. For an MDM structure to switch via this mechanism, one of the electrodes (let us call it the top electrode) must be electrochemically active (oxidizable), e.g., Ag or Cu [90], while the other electrode (the bottom electrode) must be inert, e.g., ITO or Pt (Fig. 4). When a positive voltage is applied to the top electrode, oxidation of the electrode atoms occurs, forming metal cations. The dielectric between the electrodes serves as a matrix in which electromigration of metal cations takes place under the applied electric field

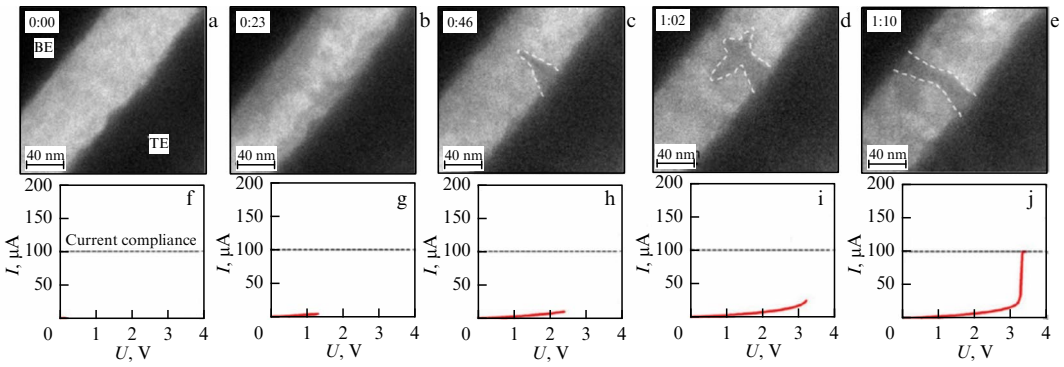

Figure 2. Series of TEM images of a ZnO film sandwiched between Pt electrodes during an increase of the applied positive bias relative to the TE electrode: (a) initial state of ZnO; (b) state under a small applied bias (contrast near both electrodes increased); (c) with increasing applied bias, a conical portion of the filament appears near the TE electrode; (d) the filament takes on a dendritic shape but still does not reach the BE electrode; (e) the filament passes through the BE electrode, and the film switches to the conducting state R_{on}; (f–j) corresponding current-voltage curves showing that switching occurs via filament formation. The dashed line in graphs (f–j) indicates the compliance current [75].

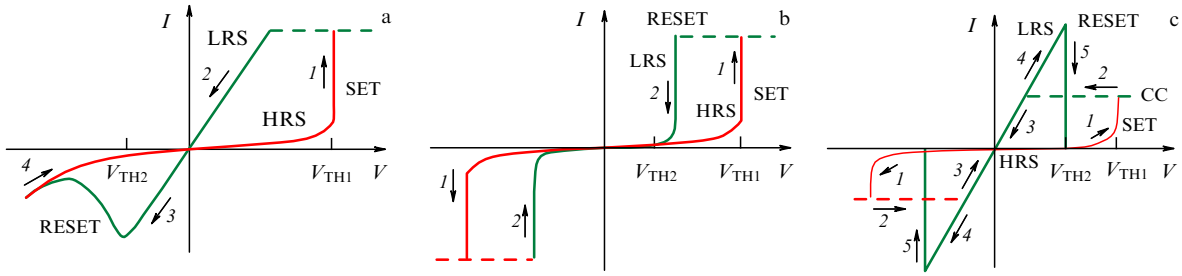

Figure 3. (a) Current-voltage characteristics of a memristor under bipolar switching, (b) unipolar switching, and (c) unipolar switching with current compliance; V_{TH1}, V_{TH2} — the switching voltages to the low-resistance state (LRS, SET operation) and high-resistance state (HRS, RESET operation), respectively [85].

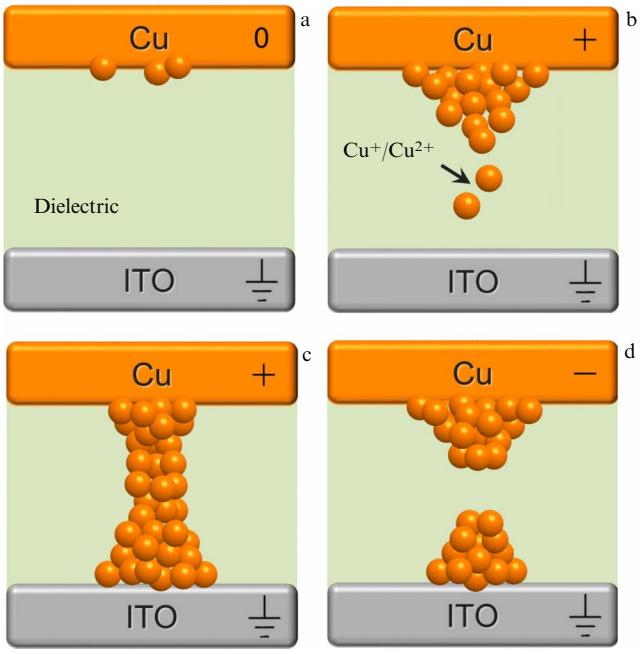

Figure 4. Scheme of the operating principles of ECM memristors: (a) initial state of the MDM memristive structure; (b) application of a positive bias to the top electrode leads to electromigration of metal cations through the dielectric matrix and the formation of a metallic filament nucleus on the bottom electrode; (c) at a sufficiently high bias (above the metal reduction potential), the metallic bridge connects the two electrodes, and the memristive structure switches to the R_{on} state; (d) application of a reverse polarity bias leads to the rupture of the metallic bridge and a return to the R_{off} state [91].

(Fig. 4b). Upon reaching the bottom electrode, the metal cations are reduced there, forming a metallic bridge (filament) between the two electrodes, which switches the memristor to the R_{on} state (Fig. 4c). When a reverse polarity bias is applied to the top electrode, the thinnest part of the conductive filament is disrupted due to Joule heating and/or the electron wind effect (Fig. 4d) [92]. Some of the cations then return to the top electrode, and the memristive structure switches to the R_{off} state.

Memristive structures in which switching occurs due to a phase transition of the active layer (phase change memory, PCM) are most often fabricated using chalcogenide materials, such as $Ge_2Sb_2Te_5$ [93, 94]. When unipolar voltage pulses are applied and, consequently, Joule heating is released, PCM materials exhibit a reversible transition from the amorphous phase to the crystalline phase, which have different resistances [95, 96]. When a voltage exceeding the threshold U_0 required to initiate melting in the active layer is applied to the device, localized melting occurs inside the chalcogenide material, leading to a transition to the amorphous phase and switching to the high-resistance state. Conversely, if the applied voltage is below U_0, gradual crystallization of the material occurs due to Joule heating, which enables switching to the low-resistance state. It is also possible to obtain intermediate resistance states of the PCM memristor lying between R_{on} and R_{off}. It is worth noting that PCM structures can also be switched by laser pulses or sufficiently intense light pulses for the realization of optical neuromorphic computing systems [97, 98].

The operation of memristors with a ferroelectric tunnel-transparent active layer (ferroelectric tunneling junction, FTJ) is associated with the ability to change the electrical polarization of ferroelectrics by applying an external electric field. The polarization of the material depends on the polarization history and is retained in the absence of an external electric field. When an electric field is applied, macroscopic regions of the ferroelectric with the same direction of dipole moments (domains) orient themselves along the direction of the applied field. By reversing the polarity of the external electric field, the polarization of the resulting ferroelectric monodomain can be rotated by 180°, yielding two distinct polarization states of the ferroelectric. The switching of ferroelectric polarization in an FTJ structure alters the height of the tunneling barrier for electrons passing through the ferroelectric layer, and consequently changes the resistance of the structure. The R_{off} and R_{on} values of FTJ structures differ by several orders of magnitude [99–101]. Doped HfO_2, $Hf_{0.5}Zr_{0.5}O_2$ or $HfAlO_x$, and perovskites are often used as ferroelectrics [102–105]. In recent years, a more optimal FTJ device structure, metal–van der Waals ferroelectric–graphene, has been proposed, which helps to overcome the challenging problem of controlled barrier modification at the metal–ferroelectric interface [106, 107].

In memristors based on the spin-transfer torque (STT) effect, two ferromagnetic layers are used, separated by a tunnel-transparent dielectric spacer (crystalline MgO often serves as spacer [108]). One of the magnetic layers has a fixed magnetization orientation, while the other layer, which is magnetically soft, can easily switch its magnetization between two opposite orientations of the magnetic moment [109]. By passing a spin-polarized current through the tunnel junction, the magnetization orientation of the magnetically soft layer can be changed. The resistance of the structure is low if the magnetizations of the layers are aligned in the same direction and increases when the magnetizations are oriented opposite to each other.

3. Basic parameters of memristors for neuromorphic computing

The main parameters of memristors that determine the effectiveness of their application in NCS include the variation in resistive states both cycle-to-cycle (C2C) and device-to-device (D2D), the maximum number of distinguishable states (plasticity) and their retention time, the resistance range (R_{off}/R_{on}), the maximum number of cyclic RS operations without significant degradation (endurance), the switching speed and the energy consumption, the minimum device size, scalability and compatibility with modern silicon technological processes. For the creation of large transistor-controlled memristor arrays, low switching voltages of individual devices (< 3 V) and a sufficiently high-resistance in the ON state (> 10 kΩ) play an important role.

The variation in the resistive states of memristors (high-resistance, low-resistance, and intermediate states), associated with the stochastic nature of the processes governing RS, is one of the key problems limiting the use of memristors in neuromorphic computing (for example, for some tasks, a 5% uncertainty in setting the resistive state can completely disrupt training convergence) [110]. For instance, in memristors switching via the valence change mechanism or electrochemical metallization, the variability in R_{on} and R_{off} values is associated with random atomic rearrangements during filament formation/rupture, filament branching due to competition between ion migration and electrostatic forces, filament formation at random points of maximum field strength, and nonuniform electrode — active layer contact. This leads to a resistance value variation of 9–10% (estimated as twice the ratio of the sum of the standard deviations of the logarithms of the resistances in the extreme states to the difference between their mean logarithms [73]) during cyclic switching [111]. Approximately the same variation of values is observed in PCM memristors [112]. In case of PCM memristors, the cause of parameter variation is the stochastic nature of the crystallization–amorphization process, associated with uncontrolled melt cooling rates and the sizes of crystalline phase nuclei. STT memristors exhibit the smallest resistance variation ($< 1\%$) [113].

Plasticity, i.e., the ability of memristors to smoothly and reversibly change their resistance between the extreme states R_{on} and R_{off} in response to external stimuli (voltage, current), is of fundamental importance for emulating the analog behavior of biological synapses [114]. Several switching algorithms for setting a memristor to a desired resistance state have been proposed in the literature. One of them consists of using additional circuit elements, in particular resistors [115], which act as a voltage divider. Although this switching method enhances robustness against cyclic resistive switching [116], its significant drawbacks include indirect control of the resulting memristor resistance and the use of additional circuit elements, which increases power consumption, hardware costs, and chip area. Another method for switching a memristor to a desired resistance state is based on applying voltage pulses with gradually increasing amplitude [117]. In this method, the resistance of the memristor is brought close to the target value by increasing the amplitude of applied pulses of fixed duration by a small amount. The sign of the pulse amplitude is determined by the sign of the difference between the current resistance and the target value. Variations of this method, based on randomly varying pulse duration [118] or fine-tuning of the resistive state using small-amplitude pulses [30], allow for improved accuracy in setting the desired state. At the same time, modulation of the amplitude and/or duration of pulses also leads to a significant overhead in processor hardware resources. In this regard, the most suitable method for setting resistance values appears to be applying a series of short consecutive pulses of the same amplitude and duration to the memristor, gradually changing its resistance. This approach yields so-called long-term potentiation curves (conductance increase as a function of the number of applied pulses) and long-term depression curves (under a series of pulses that gradually transition the memristor to R_{off}) [73]. However, this approach requires very low variation in the SET and RESET voltages, since voltage pulses with hardware-fixed parameters (amplitude and duration) may not be suitable for all elements of a memristor array.

To determine the retention time of intermediate states, a memristor is switched to the target intermediate state, the write/erase voltage is removed, and the resistance is then measured at fixed time intervals. In this case, the time during which the resistance changes (spontaneously, i.e., under the influence of internal dynamic processes) by more than 10% from its initial value is recorded. To extrapolate the retention time, measurements are performed at elevated temperatures. The dependence of retention time on temperature follows the Arrhenius law. Based on such extrapolation, the retention time of the best memristors can reach 10 years or more [119].

For memristors switching via the valence change mechanism or electrochemical metallization, the retention time depends on the activation energy of ion migration [33, 45]. In PCM memristors, the key factor is the crystallization activation energy [120]. The higher the crystallization activation energy, the longer the state is retained. High anisotropy of the free layer (e.g., CoFeB) increases the retention time in STT memristors [18]. In ferroelectric memristors, the main factor affecting the retention time is the magnitude of the coercivity [106].

A large number of intermediate states (more than 50) and long retention time (extrapolated retention time of more than 10 years) are exhibited by VCM and ECM memristors (with a tendency toward longer retention time for VCM devices), as well as PCM memristors (extrapolated retention time of ~ 10 years and more than 15 states) [119, 121]. A significantly smaller number of intermediate states is characteristic of FTJ and STT memristors, with FTJ devices also having a short retention time (on the order of 2–3 days).

Significant differences between R_{on} and R_{off} values enable a larger number of intermediate resistance states of the memristor and, thereby, a considerable number of possible synaptic weights when used in NCS. Quite high R_{off}/R_{on} ratios are demonstrated by FTJ devices ($R_{off}/R_{on} > 10^7$) and ECM memristors ($R_{off}/R_{on} > 10^5$) [106, 122]. PCM and VCM memristors also exhibit a good resistance range, with R_{off}/R_{on} ratios lying in the range of 10^2–10^4 [123, 124]. STT memristors have the lowest R_{off}/R_{on} ratios.

Another important parameter of memristors for their applications in NCS is the endurance to cyclic RS. Endurance is defined as the maximum number of switching cycles for which the resistance window between the high-resistance and low-resistance states (R_{off}/R_{on} ratio) or, for example, between an intermediate state and the low-resistance state is maintained [125].

The limitation on the number of stable resistive switching cycles is related to structural 'fatigue' of the material. This is

particularly pronounced in redox systems and phase-change systems. In redox systems, irreversible changes in resistance values during cyclic switching are associated with undesirable redox reactions at the electrodes, uncontrolled filament growth, and unwanted atomic diffusion [126]. In the case of PCM memristors, phase segregation occurs within the melt, and mechanical stresses arise during crystallization–amorphization processes, which can lead to the formation of structural defects [127, 128]. Spin-transfer torque memristors exhibit greater durability due to the electronic mechanism of resistive switching (without ion migration during switching) [73]. For all types of memristors considered in this paper, except ferroelectric ones, the number of switching cycles for the best representatives of each class exceeds 10^{11}–10^{12} [113, 129, 130]. In FTJ memristors, the reported number of RS cycles does not exceed 10^7 [131].

Low switching energy and high switching speed are advantageous for almost all types of computing, especially for applications requiring frequent device programming. The switching speed in memristors is determined by the structure of the materials, the physical mechanisms of resistive switching, and external conditions (applied voltage, temperature) [73]. In VCM and ECM memristors, the switching time is most often limited by the ion diffusion rate (the RS time is inversely proportional to the diffusion coefficient). In PCM memristors, the switching time depends on the nucleation and growth rate of the crystalline phase, while in STT and FTJ memristors, it depends on the rate of change of magnetic and electric polarization, respectively. Since changing magnetic polarization requires minimal atomic displacements, STT memristors generally require low switching energy. In VCM and ECM memristors, the energy consumption strongly depends on the activation energy of ion migration: for material with the higher the activation energy the more energy is required for switching.

The switching energy consumption of modern VCM, ECM, PCM, and FTJ memristors is about ~ 100 fJ [132–134]. For STT memristors the switching energy can be reduced to 10 fJ [135]. The highest switching speed (< 90 ps) is achieved in VCM memristors [136]. In PCM memristors, switching speeds of ~ 700 ps can be attained, and in STT memristors ~ 200 ps [137, 138]. The lowest speed is exhibited by FTJ memristors, whose switching time typically exceeds 10 ns [132]. However, it should be noted that, generally, the memristors with higher the switching speed exhibit the shorter the retention time of the resistive states and the lower the cyclic endurance. This is due to the aforementioned energy-activated mechanism of resistive switching, and practical use requires finding an optimal balance of the corresponding characteristics.

High integration density of elements increases portability and reduces the cost of NCS. The scalability of memristors is a key advantage that makes them promising for post-silicon electronics. For instance, crossbar structures based on HfO_2/TiO_x with a critical dimension of 2 nm and a half-pitch between elements of 6 nm have been demonstrated [139]. Furthermore, memristive devices based on TaO_x have been integrated into integrated circuits with a memory capacity of 7.2 Mbit and a critical dimension of 22 nm [140]. In most cases, ECM devices are scalable due to their localized conduction channels. Scalability of phase-change memristors has been achieved using carbon nanotube electrodes with a contact area of ~ 5 nm^2 [134, 141]. For STT memristors, megabit-scale integration has been demonstrated using 22-nm and 28-nm technological processes, with the possibility of scaling to dimensions below 10 nm [142–144]. Ferroelectric memristors based on $BaTiO_3$ can be miniaturized to 20 nm using Ag nanoisland electrodes [145]. The possibility of creating 3D memristive structures has also been demonstrated: 8-Layers 3D vertical crossbar arrays based on $TiN/HfO_2/TaO_x/Ti/TiN/W$ have been fabricated [146, 147]. It should be noted that downscaling of memristive devices generally leads to reduced power consumption [148]. Key problems in memristor downscaling include local overheating due to high power density, electrostatic interference, and increased parameter variation. Moreover, it is important that the main parameters are achieved specifically for CMOS integrated memristive devices. This requirement is necessary because underlying CMOS transistor layers of the NCS integrated circuit are still most often used to control memristors (ReRAM memory cells) and to perform auxiliary logic operations and switching in NCS [149].

4. Main methods of parameters' optimization of neuromorphic computing systems on memristors

Every year a considerable number of new memristors operating within one of the above-described RS mechanisms are created. Researchers select increasingly optimal materials and more sophisticated structures, relying on developed models of memristor operation. Unfortunately, to date, despite the diversity of memristive devices, there is still no memristor that, from a practical standpoint, is suitable in all its characteristics for implementation in NCS. Among the main approaches to improving the performance of memristor-based NCS, one can highlight the design of memristor materials and structures, and the development of new circuit solutions and architectures of neuromorphic systems. The first approach aims to create memristive systems with optimal parameters for use in NCS, while the second is associated with reducing the negative impact of memristor imperfections on the efficiency of NCS operation. Let us consider these approaches in more detail, focusing mainly on the improvement of memristor materials and structures.

One method for improving memristor parameters is defect engineering. For example, creating dislocations in memristive structures allows controlling the localization of filament growth and thereby reducing the spread of memristive characteristics. In this case, specific channels appear within the memristive structure with a much higher diffusion coefficient for conducting ions than in the surrounding matrix [150, 151]. Filament growth occurs predominantly along these channels, which stabilizes the memristive parameters. In this way, highly reproducible resistive switching can be achieved, and the dispersion of switching voltages can be as low as 1% [151].

Improving memristor performance can also be achieved through doping [152–154]. For instance, in the case of a zinc oxide based memristor, the R_{off}/R_{on} ratio can be significantly increased by introducing Cr atoms into ZnO [152]. The authors of [152] attribute this to a change in the oxygen vacancy concentration in ZnO resulting from doping.

In the case of metal oxide memristors, the formation of defects such as oxygen vacancies alters the oxide stoichiometry, allowing control over the memristor characteristics. One way to vary the oxygen vacancy density is ion irradiation. In [155], numerical simulation showed that radiation irradiation

of oxide based memristors with α-particles significantly changes the synaptic weights in a neural network with memristive synapses, enabling optimization of its characteristics. Experimental confirmation of a substantial improvement in the characteristics of titanium dioxide based memristors as a result of α-particle irradiation is demonstrated in [156]. It was shown that α-particle irradiation leads to an almost three-fold increase of the plasticity of memristor, the R_{off}/R_{on} ratio increases more than twofold, and the endurance increases by a factor of 1.5.

Another method for optimizing memristor parameters is to use materials with a porous structure as the active layer of VCM and ECM memristors. During switching in such memristors, a filament between the two electrodes is formed/ruptured. The thinner the formed filament, the lower the currents required for its formation/rupture and, consequently, the lower the power consumption of such memristors. On the other hand, thin filaments are unstable and easily change their morphology during RS, gradually broadening and growing. The porous structure of the memristor active material can act as a filament width limiter, guiding and controlling them. Zeolites, for example, can serve as the porous material. Thus, in [157], an Ag/LTA–zeolite/Al structure switching via the electrochemical metallization mechanism was investigated. To better control RS, metal bridge (filament) nuclei — Ag^+ cations — were added to the zeolite. Ag clusters then formed in the zeolite pores. When a positive bias is applied to the top electrode of such memristors, cations from it diffuse through the zeolite pores and are reduced on the Ag clusters, gradually filling the pores and forming a metallic bridge connecting the electrodes (Fig. 5a). On the other hand, when a reverse polarity bias is applied, the bridges are disrupted. Isolated Ag clusters remain in the pores, and the memristor returns to its initial high-resistance (Fig. 5b) or intermediate state (Fig. 5c). In this way, the morphology of the metallic bridges can be controlled, preventing their uncontrolled growth (in this case, the pore openings are only 0.41 nm). Thanks to such a structure, the power consumption of Ag/LTA–zeolite/Al memristors is less than 10 fJ.

High-entropy multi-metallic (consisting of a mixture of five or more metals) oxide systems can serve as the active layer of a VCM memristive structure to reduce the stochasticity of memristive characteristics and increase the retention time of resistive states and the endurance of memristors [158]. Since each element of such an oxide system has its own crystal structure, their mixing produces a quiet strongly distorted lattice. Oxygen vacancies diffuse extremely slowly through such a lattice, leading to an increase in the retention time of resistive states (> 20 h at 100 °C) and a large number of stable states over time. Moreover, because high-entropy oxides contain elements of various valences, these oxides are electrically neutral, and oxygen vacancies are uniformly distributed throughout the active layer of the memristive structure. The uniform distribution of vacancies leads to a reduction in the variability of memristive characteristics (switching voltage dispersion ~ 7%).

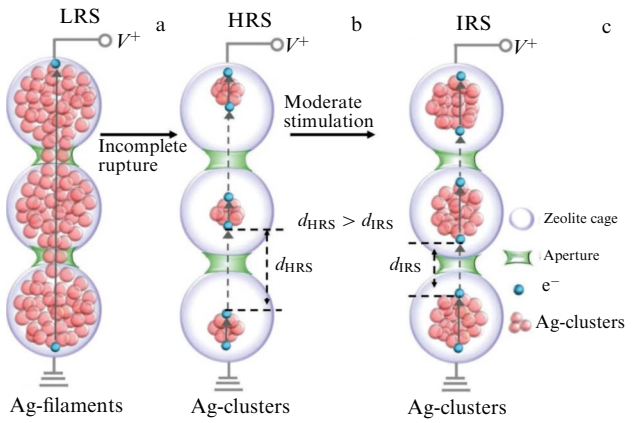

Figure 5. Scheme of the Ag/LTA–zeolite/Al memristor in states (a) R_{on}, (b) R_{off}, and (c) an intermediate state [157].

The stability of resistive switching increases when a thin metallic buffer layer, e.g., Cr, Pt, Cu, is introduced into the main dielectric layer of the memristive structure [53, 159, 160]. In this case, a defective interfacial layer may form between the introduced metallic layer and the main dielectric layer of the memristor, affecting the charge carrier transport into it [159]. Furthermore, the introduction of a metallic layer reduces the thickness of the dielectric layer in which RS occurs, which also stabilizes the memristive characteristics, for example, reducing switching voltages and their dispersion [53, 159].

In the case of metal–nanocomposite–metal structures based on metal oxide nanocomposites, the transition to the conducting state is determined by percolation pathways defined by the spatial position and concentration of metal nanogranules in the composite matrix. Therefore, the endurance to RS in this case is high, and the RS mechanism is multifilamentary [47, 160, 161].

The metallic layer can also act as a diffusion barrier for cations in ECM memristors. With 'fast' diffusion of cations from the top electrode, an excessive number of conducting bridges and/or excessively thick bridges can form, which are difficult to rupture and switch the structure to the R_{off} state. Therefore, for example, a thin Ta layer can be used to limit the injection of Cu cations into the dielectric layer of the $Cu/HfO_2/Ta/Cu_2S/W$ structure (Fig. 6) [161]. In such a memristive structure, resistive states can be set with good accuracy by limiting the maximum current through the structure (average dispersion of R_{on} resistive states obtained at different compliance currents ~ 10%). This approach also works for organic ECM memristors [162].

Not only modification of the active layer but also changing the composition of the metal electrodes can lead to optimization of memristor parameters. Using an Hf–In–Sn–O composite instead of indium tin oxide (ITO) as the top electrode in zinc oxide based memristors reduces power consumption, increases the stability of memristor operation, and improves the R_{off}/R_{on} ratio [163, 164]. Furthermore, studies [165, 166] have shown that, in addition to the bottom electrode material, the adhesive metal layer plays an important role in the stability of resistive switching.

An effective method for improving memristor parameters is the incorporation of nanoparticles into the active layer [47]. Nanoparticles can act as charge trapping centers [167, 168]. For instance, in memristors based on Ni–Au nanoparticles, nickel readily oxidizes in air, creating oxygen vacancies on the nanoparticle surface [167]. Under an applied external bias, these vacancies can give rise to an additional uncompensated charge, altering the Schottky barrier at the interface between the insulating phase layer containing nanoparticles and the bottom electrode (in this case, Nb doped $SrTiO_3$) and switching the memristor to the R_{off} state. When a reverse polarity bias is applied, the oxygen vacancies become ionized,

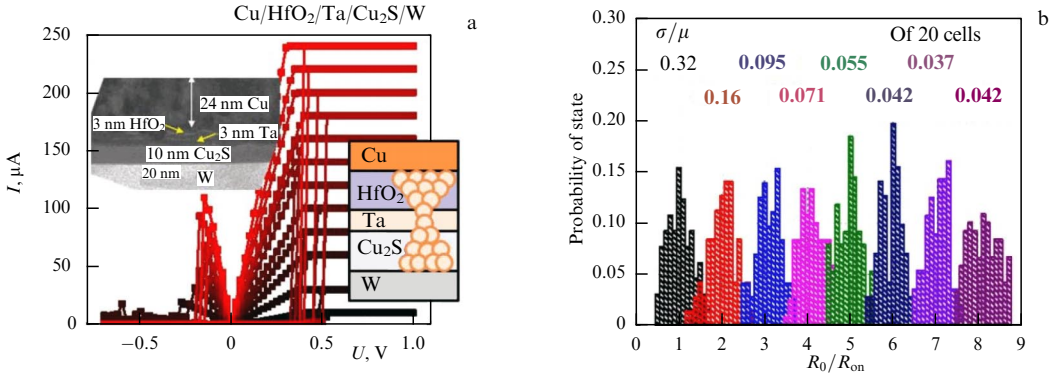

Figure 6. Memristive structures based on $Cu/HfO_2/Ta/Cu_2S/W$: (a) typical $I-V$ characteristics with images of the structure (schematic and TEM images); (b) distributions of R_{on} when set with different compliance currents (R_0 — quantum of electrical resistance or von Klitzing constant, approximately 12.9 kΩ) [161].

leading to a narrowing of the Schottky barriers and switching to the R_{on} state. A similar resistive switching mechanism is observed in some other structures, for example, in a structure based on colloidal zinc oxide nanoparticles in a polymer matrix [169].

Furthermore, metal nanoparticles can act as electric field concentrators in the dielectric layer, setting and fixing the direction of filament formation (in VCM memristors) or metallic bridge formation (in ECM memristors). Thus, incorporating a layer of Pt nanoparticles into a TiO_2 layer reduces the dispersion of the SET voltage U_{set} from $\sim 60\%$ to $\sim 10\%$, and also increases the retention time of resistive states [170]. In structures based on the nanocomposite $(Co–Fe–B)_x(LiNbO_3)_{1-x}$ with a pure $LiNbO_3$ interlayer, it has been shown that high reproducibility and multilevel RS are achieved through the formation of percolation chains of metallic nanogranules, which spatially fix the location of the filaments [54, 171, 172].

The improvement of memristor parameters can also be achieved by incorporating a uniform layer of metal nanoparticles or homogeneously distributed nanoparticles ordered within the active layer [173–178]. Reference [173] emphasizes that incorporating a Ru nanoparticle layer into an Al_2O_3 layer reduces the dispersion of R_{off} resistances from 76% to 13%. Additionally, homogeneous metal nanoparticles can be embedded in close proximity to the top or bottom electrode, thereby creating nuclei for metallic bridges [174].

One of the approaches to combating parameter variation in VCM memristors is the use of multilayer structures (stack engineering). The idea is to try to confine all stochastic mechanisms as much as possible by splitting the switching process into several parts through the creation of multilayer materials. To reduce stochastic parameter variation, structures such as $HfO_x/TiO_x/HfO_x/TiO_x$ [179], $HfO_x/Ti/HfO_x/Ti$ [127, 180], $Pt/Al_2O_3/HfO_2/TaO_xNy/TiN$ [181] and $Pt/Al/TiO_x/HfO_2/AlN/Pt$ [182] have been used. In the field of neuromorphic applications, the Al_2O_3/TiO_{2-x} combination has been successfully employed as a switching layer in a neural network for image classification [34].

In the last decade much attention has been paid to the development of memristors based on two-dimensional materials. Some studies indicate that grain boundaries present in such materials facilitate the resistive switching process [183–185]. Moreover, these materials exhibit a wide variety of electronic spectra, covering semimetallic, semiconducting, and insulating states depending on their atomic composition [186]. Two-dimensional materials can be combined into a multilayer structure. Each layer of such structure is formed by covalently bonded atoms, while van der Waals forces act between the layers [187]. The thickness of a such structure can be precisely controlled because its variation is discrete, i.e., determined by the number of layers. This configuration makes it possible to fabricate memristors with very thin insulator layers to confine stochastic processes associated with switching. This significantly helps to reduce cycle-to-cycle variability [188]. Furthermore, combining two-dimensional materials with different properties allows the desired memristor characteristics to be achieved.

Transition metal dichalcogenides, as typical 2D materials, have been extensively studied in memristor devices [189, 190]. For example, in 2015, a memristor based on MoS_2 was reported, and in 2022, MoS_2 based memristors with extremely low parameter variability were successfully used as artificial synapses [191, 192]. In 2019, a memristor based on a $MoSe_2/Bi_2Se_3$ heterostructure was fabricated. The device provided threshold switching and mimicked synaptic plasticity under near-infrared irradiation [193]. Memristors based on $MoSe_2/MoS_2$ heterostructures exhibit good bipolar resistive switching characteristics with low parameter variation and mimic synaptic plasticity [194]. A $Mo/MoSe_x/MoSe_2$ structure (where $x < 2$) with relatively stable RS parameters was also realized through controlled Se diffusion [195].

Although most research groups still focus on inorganic memristors, the resistive switching effect has also been demonstrated in structures based on organic materials: electroactive polymers, polymer blends, small organic molecules, polymers serving as matrices for organic and inorganic nanostructures, and other hybrid structures [196, 197]. Moreover, the RS mechanisms described in Section 2 are applicable to organic memristors, although there exist RS mechanisms that are predominantly characteristic of organic structures, for example, RS resulting from conformational transitions [71].

Advantages of organic memristors include low production cost, ease of fabrication, flexibility, and biocompatibility, which is promising for wearable and implantable electronics [198]. Through molecular design, the electrical, optical and mechanical properties of organic materials can be tuned, which is extremely important for creating controllable memristive structures [199, 200]. Moreover, organic memristive structures are almost on par with inorganic ones in terms of basic memristive characteristics [201]. However, organic memristors also have their weaknesses. The main disadvan-

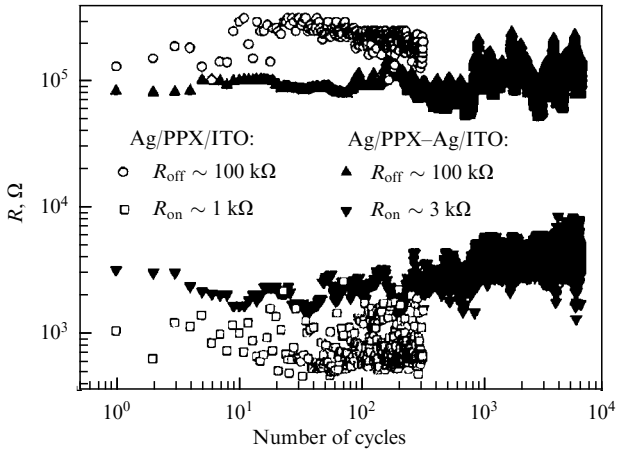

Figure 7. Endurance to cyclic switching of memristive structures based on pure PPX (open circles and squares) and PPX with silver nanoparticles (filled triangles) [170].

tages of most organic memristors include low reproducibility of characteristics from C2C and from D2D, stochasticity of resistive switching, short retention time of resistive states, relatively low R_{off}/R_{on} ratio, and lower thermal stability compared to inorganic memristors [71, 201].

As with inorganic memristors, the parameters of organic memristors can be improved by incorporating inorganic nanoparticles into the organic matrix (i.e., by creating hybrid organic–inorganic structures). Thus, studies [170, 202] have shown that embedding silver nanoparticles into poly(p-xylylene) (PPX) based memristors leads to a smaller spread of switching voltages, a greater number of stable switching cycles from one state to the other and back, as well as lower power consumption. Figure 7 shows the endurance of memristive structures based on PPX and PPX-Ag. Memristive structures with Ag nanoparticles exhibit no less than 6000 stable RS cycles from the R_{off} state to R_{on} state and back, which is more than an order of magnitude higher than that achieved for structures based on pure PPX (~ 300). The Ag metal nanoparticles in the PPX layer form percolation chains, concentrate the electric field, and set the direction of conductive bridge formation. This partially suppresses the stochastic nature of RS, increases their stability, and reduces the required switching voltage. Similar results are achieved by incorporating semiconductor nanoparticles (e.g., MoO_x, PbTe) into the PPX matrix, with the characteristic spread becoming less than 10% [56, 203].

Good results are also obtained using organic–inorganic hybrid perovskites. Conductive filaments in this type of memristor form due to the migration of halide ions (e.g., I^- and Cl^-). Halide vacancies (such as iodine vacancies) have been identified as the main type of defect associated with mobile ions (much like oxygen vacancies in metal oxide memristors). Zhu and colleagues demonstrated a $MAPbI_3$ based memory with a high R_{off}/R_{on} ratio of 10^7 [204]. They confirmed that the RS effect in the $MAPbI_3$ layer depends on the presence of iodine vacancies. Improvement of RS parameters in such systems can be achieved by appropriate selection of electrode materials. Research [205] reports the fabrication of a memristor based on $CH_3NH_3PbI_{3-x}Cl_x$. The cell demonstrated a low operating voltage of 0.1 V, long retention capability, and various stable resistance levels.

Another approach to optimizing the parameters of organic memristors involves the addition of two-dimensional layers to the structure. In 2019, the possibility of reducing the stochasticity of characteristics of PPX based memristors by introducing a graphene barrier layer was demonstrated [206]. On the one hand, the graphene barrier layer limits the diffusion of ions from the top electrode, preventing an excessive amount of metal ions from entering the PPX layer and the formation of large metallic bridges that are subsequently difficult to rupture with reverse-polarity voltage. On the other hand, since ions can diffuse into the PPX layer only through the nanopores present in the graphene structure, control over the location of the metallic bridges increases, thereby reducing RS variability.

Another common strategy for combating parameter variation in memristive devices of any type is the sequential connection of a transistor to the memristor, the so-called 1T1R memory cell (Fig. 8) [35, 63, 207–209]. The role of the transistor is to force the memristor to operate only within a narrow voltage range, minimizing the impact of variability. The transistor also makes it possible to prevent sneak path currents in a crossbar memristor array through isolated writing/reading of each individual memristor in the matrix (random addressing of elements in a ReRAM array). Complementary structures are also used, in which two memristors connected in series are paired with one transistor (1T2R), and the voltage is measured at the point between the two memristors [210]. Using this configuration, information is stored as the resistance ratio of both memristors rather than in a single device, which reduces parameter variation during cyclic switching. Furthermore, there are researchers in which more than one transistor is used to access the memristor, improving the stability and reproducibility of such devices both during their fabrication (protection against damage from ion bombardment, electrostatic discharge, etc.) and during operation (stable reproduction of multibit states, protection against temperature and field variations) [211]. Instead of a transistor, another device, a so-called selector (1S1R structure), can be used; diodes, phase-change elements, and others can serve as selectors [212–214].

It should also be noted that the improvement of certain characteristics can be achieved by using not two-terminal

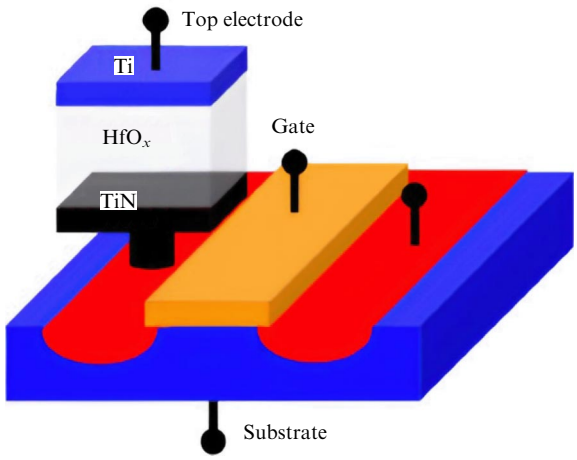

Figure 8. Scheme of a 1T1R structure. The $Ti/HfO_x/TiN$ structure as a memristor is connected in series with the source of a field-effect transistor [209].

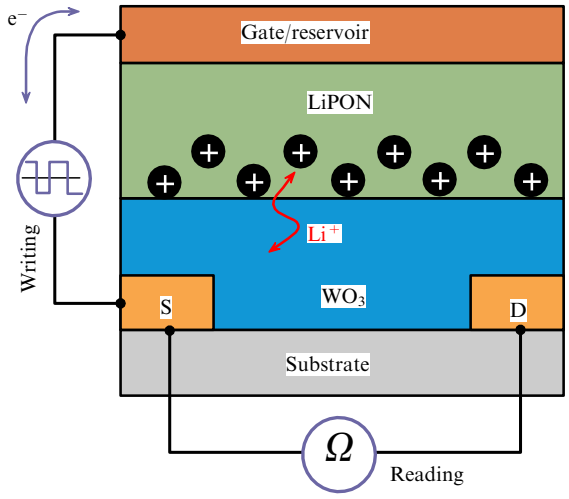

Figure 9. ECRAM with the ion movement Li^+ modulated channel conductance [215].

memristors but memristors with three electrical terminals. As an example, Figure 9 shows the structure of an electrochemical random access memory (ECRAM) consisting of a MOSFET in which the dielectric layer is a solid-state electrolyte based on lithium phosphorus oxynitride (LiPON) [215, 216]. The operation of the device is based on the intercalation/deintercalation of ions in the channel layer to tune the device conductance. Intercalation of Li^+ ions into the WO_3 layer is achieved by applying a positive bias to the gate, which increases the device conductance, while deintercalation of Li^+ ions under negative bias decreases the conductance. It is noted that organic materials such as poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) can also serve as the gate dielectric [217]. Linear conductance modulation in ECRAM is possible due to the separation of read/write paths, making this device concept very attractive for synaptic applications, primarily for hardware implementation of synaptic weights in artificial neural networks, where analog and symmetric weight updates play a crucial role. Furthermore, the device investigated in [215] provides low power consumption and fast operation on a nanosecond timescale, thereby paving the way for significant acceleration of the learning process in hardware implementations of artificial neural networks.

The variability of memristor parameters can also be compensated by designing an appropriate artificial neural network architecture. When a smaller number of memristors is used in artificial neural networks, the impact of the spread of their characteristics is reduced. The number of memristors in hardware implementations of artificial neural networks can be decreased, for example, by using convolutional networks [218], sparse coding systems [219], and reservoir computing systems [220]. Furthermore, new learning principles for NCS are being developed. Among these, one can note the training of spiking NCS using bio-inspired rules such as spike-timing (or spike-rate) dependent plasticity (STDP/SRDP) [221–224], neuron–astrocyte networks [225], and other learning methods [226]. In this case, synaptic connections are trained locally, without the need for global (dependent on the states of many neurons and network weights) and precise changes (as in the case of the back-propagation algorithm in formal NCS, i.e., based on traditional (non-spiking) neural networks). With a comparable spread of memristor characteristics, spiking NCS with STDP learning can demonstrate even higher image classification accuracy than that achieved in formal networks in NCS [76].

Also very promising for robotics and agent based intelligent systems is the hardware implementation of formal and spiking NCS within the reinforcement learning paradigm, where the NCS learns to solve a task in real time by trial and error, comparing predicted values of a certain reward function formalizing the task with the actual reinforcement signal from the agent's environment [110, 227, 228].

5. Conclusion

In the coming years, memristor technology is expected to either replace or substantially augment CMOS technologies for neuromorphic computing, enabling efficient real-time processing of large data volumes. Key device characteristics, including stochasticity, scalability, integration density, power consumption, speed, stability, and endurance, are essential for building neuromorphic computing systems that mimic the operation of the brain. As the data presented here show, individual devices have achieved excellent performance with respect to certain properties; however, overall progress across the combined set of characteristics remains limited. While memristor technology opens unique opportunities for high-performance intelligent computing, issues such as device variability and parasitic effects continue to constrain the reliable hardware implementation of neural networks. At the same time, a substantial body of experimental data has been accumulated, the underlying physical mechanisms have been uncovered, and specific technological and architectural strategies have been identified that could lead to breakthroughs in the reproducible fabrication and stable operation of reliable digital-analog neuromorphic memristor systems. Future research, including the approaches discussed in this paper as well as a number of others, may help resolve these issues within the medium term. Memristor based devices certainly hold strong promise for a wide range of practical applications.

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