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Detectors and integrated circuits of orbiting telescopes

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Contents

Abstract. Progress in X-ray astronomy is impossible without progress in X-ray detector technology. Currently, semiconductor X-ray detectors provide the best performance in terms of time and energy resolution. This paper presents a description of three types of semiconductor detectors, their sensitive elements, and specialized signal processing integrated circuits for the Spektr-RG and Gamma-400 projects and the MVN (All Sky Monitor) space experiment.

Keywords: X-ray detectors, CdTe, cadmium telluride, strip detectors, silicon detectors

1. Introduction

From 2008 to 2018, the Space Research Institute (IKI) designed several types of X-ray detectors for use in X-ray telescopes and spectrometers for space applications.

A pixel detector, D1, based on a CdTe (cadmium telluride) crystal and an integrated circuit (IC) VA32TA, was designed for the MVN space experiment (MVN is an abbreviation of Monitor Vsego Neba, the Russian transliteration for All-Sky Monitor) [1, 2], planned for installation in the Russian segment of the International Space Station (ISS). The detector is designed for X-ray spectrometry in the energy range from 4 to 120 keV and can be used in spectrometers without spatial resolution. The crystal is pixelated (32 pixels with a size of 3.7×3.7 mm) only to improve noise characteristics. The MVN scientific payload includes four D1 detectors.

A double-sided strip detector, SD01, based on a CdTe crystal and a VA64TA1 IC, was designed for the ART-XC X-ray telescope named after M N Pavlinsky [3], installed on the Spektr-RG spacecraft [4]. The detector is designed for spectrometry and imaging in the focal plane of an X-ray mirror system. The detector contains 48×48 image elements with a size of 595×595 μm and operates in the energy range from 4 to 118 keV (operating energy range of the telescope from 4 to 30 keV). The ART-XC telescope named after M N Pavlinsky includes seven SD01 detectors.

A high-speed silicon detector based on DepFET semiconductor structures and SWP1 and CAMEX PIXEL 64L ICs was designed for the Gamma-400 space project [5]. A detector prototype with a structure of 32×32 pixels and a size of 150 μm was manufactured and tested as part of the preliminary design.

The following is a brief description of the design and operation features of all three types of detectors.

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2. Detector for the MVN scientific payload

The D1 detector is shown in Fig. 1. It comprises a ceramic case, a thermoelectric module, a ceramic board, a sensitive element (SE), and a VA32TA IC.

Main technical characteristics of the D1 detector:

— overall dimensions at the base of the case is 60×48 mm;
— height is 17.5 mm;
— weight is 60 g;
— power consumption is 200 mW;
— energy range is from 4 to 120 keV;
— 'dead' time is no more than 0.7 ms;
— energy resolution (full width at half maximum (FWHM) at an energy of 13.9 keV, single events) is no more than 1.8 keV;
— geometric sensitive area is 4.38 cm^2;
— number of pixels is 32;
— pixel size is 3.7×3.7 mm;
— operating temperature is from -30 to $-20\,^{\circ}C$.

A semiconductor crystal made from ultra-pure CdTe (Acrorad, Japan) is used as an SE in the detector [6]. The crystal size is $24 \times 24 \times 1$ mm. The configuration of the electrodes on the crystal was made by Acrorad by order of the IKI. The CdTe crystal is shown in Fig. 2. The top electrode of the crystal is solid. Its Au/Pt/CdTe structure

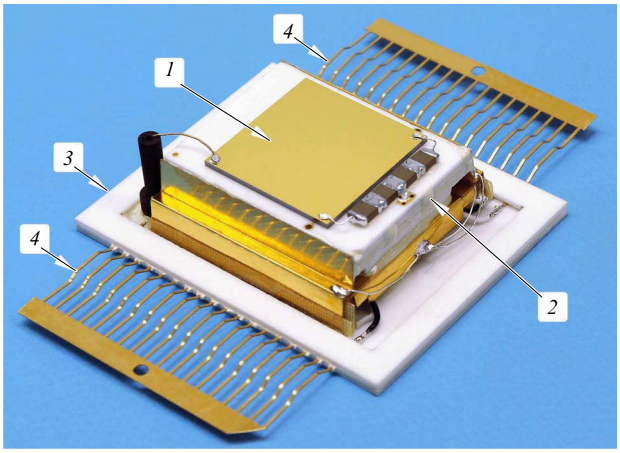

Figure 1. D1 detector (*1* — CdTe crystal; *2* — ceramic board; *3* — case; *4* — lead frame).

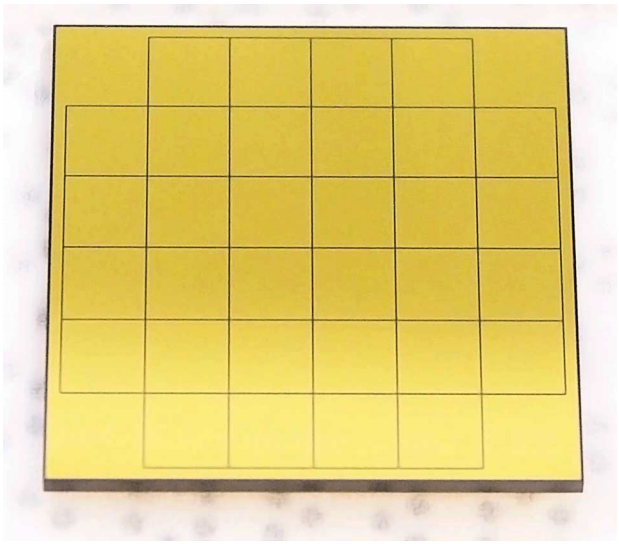

Figure 2. CdTe crystal for the D1 detector (bottom view, size 24 × 24 × 1 mm).

provides ohmic (nonrectifying) contact between the electrode and the crystal material. It is from the side of the top electrode that radiation falls on the detector. The bottom electrode is used to connect the crystal to a charge-sensitive amplifier (CSA). The bottom electrode structure is Au/Ti/Al/CdTe and forms a rectifying contact (Schottky barrier) of the electrode to the crystal material [7]. Thirty-two contact pads and a guard ring are formed on the bottom electrode by photolithography. The purpose of the bottom electrode partitioning is to reduce the parasitic capacitance of a single SE connected to the CSA. Thus, the entire volume of the crystal is divided into 32 elementary SEs (pixels) 3.7 × 3.7 mm in size, each has 32 times less electrical capacity of the whole crystal of equivalent area. The disadvantage of this solution is the increase in the complexity of manufacturing the crystal (and, accordingly, an increase in its cost), the occurrence of the effect of charge sharing between individual SEs, the need to use 32 channels instead of one channel for processing signals from the crystal, and an increase in the power consumption of the entire detector. The advantages of this solution are improved noise characteristics of the detector and increased reliability, the latter of which is achieved due to the fact that, if one of the 32 spectrometric signal processing channels fails, only 1/32 of the entire sensitive area of the detector will be lost but not the entire detector. The guard ring is necessary to reduce the contribution of the leakage current flowing along the side surface of the crystal to the total leakage current of the elementary SE.

The ceramic case is made of ADS-96R ceramic (96% Al_2O_3, CoorsTek, UK). Its purpose is to protect detector elements from environmental influences during ground operation, remove heat, and reduce mechanical stress in the thermoelectric module and ceramic board due to the difference in the thermal linear expansion coefficients between the ceramics and the case material (AMg6 aluminum alloy).

The ceramic board consists of three layers of ADS-96R ceramics. The conductive and insulating layers and resistors on the board are made using thick-film technology. A CdTe crystal is installed on one side of the board, and a VA32TA IC die and capacitors are installed on the other side. Connecting the pads on the bottom side of the CdTe crystal to the pads on the ceramic board is done using a conductive glue by the flip-chip method. The connection of the contact pads of the VA32TA IC is made using ultrasonic wire bonding technology with aluminum wire. Special attention was paid to minimizing the length of connections between the contact pads of the CdTe crystal and the inputs of the VA32TA IC when designing the ceramic board. The board is installed on a thermoelectric module (Peltier element), which is glued to the case. The thermoelectric module is used to cool the detector in ground conditions. The required temperature of the CdTe crystal is provided by the MVN thermal control system [8] when the detector operates under space flight conditions.

After installation into the instrument, the detector is closed with a hermetic protective cover. In terrestrial conditions, the hermetic volume under the cover is filled with dry nitrogen. The cover case contains the following layers: 1 mm of tin (outer layer), 1 mm of copper, 2 mm of aluminum alloy AMg6 (inner layer). This three-layer protection with materials of successively decreasing atomic numbers is used to successively reduce the energy of fluorescent X-ray photons generated in the cover material. The cover also includes an X-ray transparent, vacuum-tight beryllium window with a thickness of 100 μm and a diameter of 36 mm (Kompozit, Russia), which is the entrance window of the detector.

The electrical circuit for connecting the SE to the input of the CSA is shown in Fig. 3. The detector uses a so-called AC-connection circuit, which has worse noise characteristics than the DC-connection circuit due to the presence of an additional resistor, but the advantage of this circuit is that it can operate in a wide range of SE leakage currents. This feature makes it possible to use in the detector both an SE based on CdTe crystals with a Schottky barrier and an SE based on CdTe crystals without rectifying electrodes, which have a leakage current that is two orders of magnitude higher. In addition, the reliability of the detector increases, since an evolution of the leakage current of the crystal is possible both from changes in its electrical properties over time and from operation under conditions of exposure to charged particles in space. The circuit used is capable of automatically withstanding these changes within a fairly wide range.

VA32TA IC (Ideas, Norway) [9, 10] is a 32-channel signal processing system for semiconductor detectors. The IC is manufactured using the 0.35-μm CMOS process (AMS,

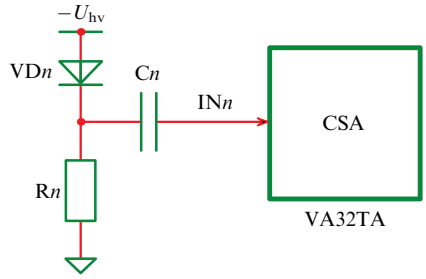

Figure 3. Connecting circuit of the SE to the input of the CSA in the VA32TA IC (n is the number of the elementary SE).

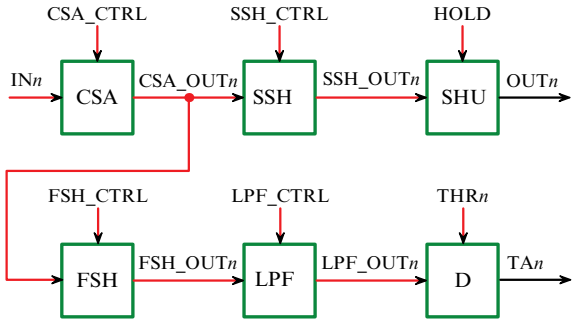

Figure 4. Block diagram of one signal processing channel in the VA32TA IC.

Austria). The IC die size is $7.035 \times 3.385 \times 0.725$ mm. A block diagram of one signal processing channel of a semiconductor detector is shown in Fig. 4. The channel consists of a CSA, a slow shaper (SSH), a sample and hold unit (SHU), a fast shaper (FSH), a low-pass filter (LPF), and a discriminator (D). The FSH provides two shaping times (37.5 or 75 ns). The shaping time of the SSH can be adjusted in the range from 0.75 to 1.5 μs. Since the IC uses a shaper with a CR-RC structure, the peaking time (i.e., the time to reach the maximum of the shaped signal) is twice as long as the shaping time. The power consumption of one channel is 6.25 mW.

A configuration memory with a capacity of 199 bits is used to store the configuration of the IC. To protect against single event upsets, each flip-flop is built using a triple modular redundancy architecture [11]. If a single event upset occurs in one of the flip-flops of the configuration memory, the IC generates a signal 'SEU,' according to which the external controller must rewrite the IC configuration memory. Configuration memory allows you to:

— control the value of the CSA feedback resistor;

— control the shaping time of fast and slow shapers;

— set a discriminator threshold common to all channels;

— adjust the discriminator threshold in each of the 32 channels;

— enable (disable) the generation of a trigger signal from any channel;

— control the polarity of the input signal.

In addition to the configuration memory, the IC has several inputs for reference voltages, which allow you to change the settings of the analog blocks of the IC and partially duplicate the functions of the configuration memory. The use of external reference voltages makes it possible to change the parameters of IC blocks within a wider range than when using configuration memory, but require the use of external digital-to-analog converters, which complicates the system.

A special feature of this IC is the absence of a peak detector in the signal processing channels. This leads to certain difficulties in obtaining information about which channel the photon was registered in. In general, the algorithm for working with the detector includes the following phases.

Before starting observations, the external controller:

— supplying the detector with the necessary reference voltages;

— loading the IC configuration memory;

— testing the detector.

Testing the detector consists of generating an artificial trigger signal, storing the current signal amplitudes in the SHU, and then digitizing them. The purpose of this procedure is to determine the magnitude of the constant signal component in each channel and its deviations. Since the output signal of the channels is well described by a normal distribution, the mathematical expectation and dispersion are determined for each channel using an ensemble of samples. The mathematical expectation corresponds to the constant component (or podium) of the output signal. The dispersion gives information about the magnitude of the noise voltage component in the output signal. Using the dispersion value, software thresholds are calculated. Obtained values of podiums and software thresholds are stored by an external controller.

In observation mode, the detector is operated according to the following algorithm. If in one of the channels the output voltage of the FSH (signal 'FSH_OUTn'), after passing through the low-pass filter (signal 'LPF_OUTn'), exceeds the threshold voltage (signal 'THRn', the hardware threshold of this channel), then the channel will issue a trigger signal with the predefined duration (signal 'TAn'). The 'TAn' signals of all channels are combined in the IC according to the 'wired OR' circuit, and the active level of any of them leads to the 'TA' signal output common to the entire IC in the external controller. After receiving the 'TA' trigger signal, the controller waits a time equal to the SSH peaking time and assign a 'HOLD' signal, which holds the current value of the SSH voltage in all IC channels. Next, the 32 signal amplitudes stored in the SHU are digitized using the IC output multiplexor. After receiving the digital values of the signal amplitudes, the external controller begins their software processing. For each received signal amplitude, the following operations are performed:

— the shifted signal amplitude is determined by subtracting the podium value determined at the testing phase from the signal amplitude;

— the shifted amplitude is compared with the value of the software threshold;

— if the shifted amplitude is greater than or equal to the software threshold, it is used to further search for the triggered channel.

Next, all shifted signal amplitudes that successfully passed the test at the first phase are compared with each other, and the number of the IC channel in which the maximum signal is obtained is determined. If the maximum value (the same) is obtained in several channels, the IC channel with the lowest number is considered to be triggered. As a result, the photon registration time, the number of the triggered channel N_0, and the signal amplitude E_0 in it are stored in a data block describing the event. In addition to the specified information, the amplitudes of signals $E_1 - E_4$ in four channels (SEs) surrounding the triggered channel (SE) are stored in the same

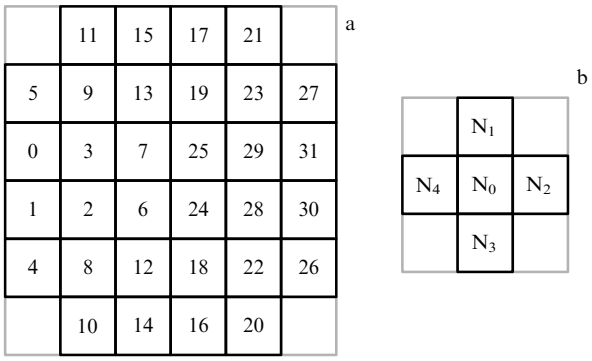

Figure 5. (a) SE numbers on a CdTe crystal (look 'through' the crystal towards radiation source); (b) location of SEs, the signal amplitudes of which are stored in a data array for further processing.

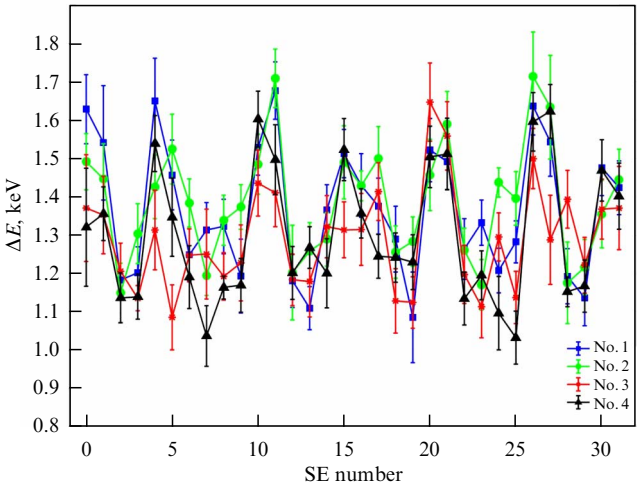

Figure 6. Dependence of energy resolution ΔE (FWHM at an energy of 13.9 keV) on SE number for four detectors D1 (−21 °C, −100 V).

data array. The layout of the SEs over the area of the CdTe crystal is shown in Fig. 5a. The layout of the SEs N_1-N_4 surrounding the triggered SE N_0 is shown in Fig. 5b. Storage of signal amplitudes in neighboring SEs is necessary for the correct restoration of photon energy in the case of charge sharing between SEs with a common boundary. On a square grid, the triggered SE is bordered by eight other SEs, but the contact area of the central SE with the diagonal SEs is very small, so, to reduce the amount of generated telemetry information, we decided to additionally store only the amplitudes of neighboring SEs orthogonal to the triggered SE. At the same time, depending on the task, it is possible to save nine amplitudes or all 32 amplitudes.

The designed algorithm for working with the detector, using software thresholds proportional to the noise voltage, makes it possible to automatically prevent an increase in the generated telemetry information and overload of the telemetry system in case of increasing noise in one of the channels.

The energy resolution of the detector was estimated from the spectrum of a ^{241}Am calibration source. Figure 6 shows the dependence of the energy resolution (FWHM at an energy of 13.9 keV) versus the SE number (IC channel). To determine the energy resolution, only single events were used, i.e., such events for which the amplitudes E_1-E_4 are less than the

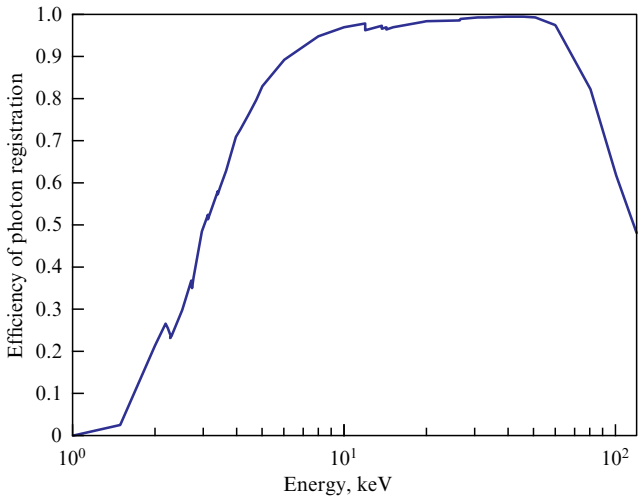

Figure 7. Dependence of efficiency of photon registration by a CdTe crystal on energy (Be (100 μm) and Au (82 nm) layers in front of the crystal).

software threshold, and the photon energy is determined only through the amplitude E_0. The degradation of the energy resolution in individual SEs is related to these SEs being located on the periphery of the crystal and having a common boundary with the guard ring (see Fig. 5). The interaction of a photon with the detector material at the boundary of the SE and the guard ring leads to the division of the generated charge between those elements. The fact that in this case the fraction of charge (signal amplitude) collected by the guard ring is unknown and the photon energy value is calculated only from the signal amplitude E_0 and the SE has not collected all of the generated charge leads to an underestimation of the photon energy. As a result, for such events, the peaks in the spectrum broaden towards low energy, which leads to a degradation of the energy resolution in peripheral SEs.

The efficiency of photon registration by a CdTe crystal versus energy is shown in Fig. 7. Efficiency is calculated assuming that there is a 100-μm-thick beryllium window in front of the crystal and a metallization thickness on the crystal equivalent to 82-nm gold.

Currently, the flight model of the MVN has been delivered to PAO S P Korolev Rocket and Space Corporation Energia (Russia), has been tested at comprehensive test bench, and is ready to be sent to the ISS. The launch of the MVN to the ISS on the Progress cargo spacecraft is planned for 2024.

3. Detector for the ART-XC telescope named after M N Pavlinsky

The SD01 detector is shown in Fig. 8. The detector consists of an SE, a crystal holder, a ceramic case, two ceramic boards, a VA64TA1 IC, and flexible printed circuit boards.

Main technical characteristics of the SD01 detector:

— overall dimensions at the base of the case are 123 × 104 mm;
— height is 19.3 mm;
— weight is 130 g;
— power consumption is 28 mW;
— energy range is from 3 to 118 keV;
— 'dead' time is no more than 0.9 ms;

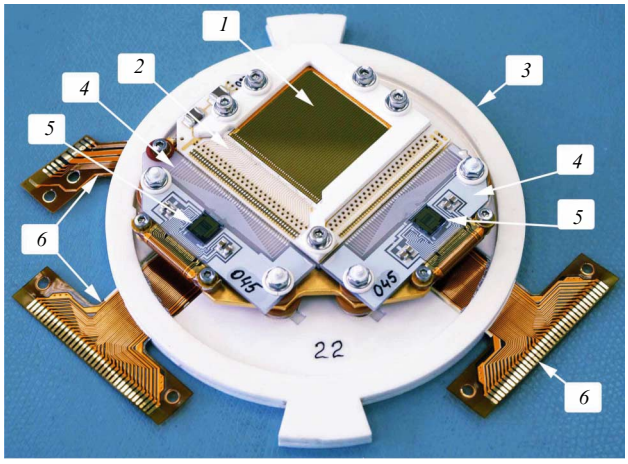

Figure 8. SD01 detector (*1* — SE; *2* — crystal holder; *3* — ceramic case; *4* — ceramic board; *5* — VA64TA1 IC; *6* — flexible printed circuit board).

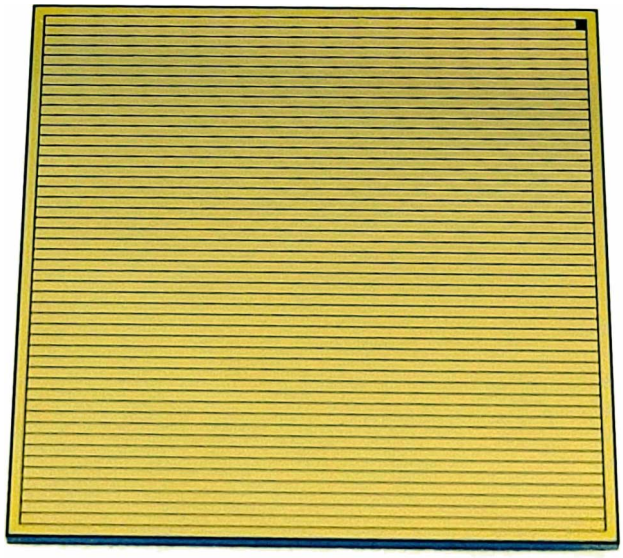

Figure 9. CdTe crystal for the SD01 detector (top view, size: 29.95 × 29.95 × 1.00 mm).

— energy resolution (FWHM at an energy of 13.9 keV, single events) is no more than 1.8 keV;
— number of strips is 48 × 48;
— size of the elementary SE (pixel) is 0.595 × 0.595 mm;
— geometric sensitive area is 8.11 cm^2;
— operating temperature is from −30 to −20°C.

The SD01 detector also uses a CdTe semiconductor crystal (Acrorad, Japan) as an SE, which differs from the D1 detector crystal in the configuration of the electrodes. The crystal size is 29.95 × 29.95 × 1.00 mm. A CdTe crystal is shown in Fig. 9. The electrodes on the crystal have a double-sided strip configuration. On the top side of the crystal, the electrode pattern consists of 48 parallel strips surrounded by a guard ring. The same pattern, but rotated 90 degrees relative to the pattern on the top side, is found on the bottom side of the crystal. The strip width is 520 μm, and the strip pitch is 595 μm. The electrodes on the top side have an Au/Pt/CdTe structure (ohmic contact) and on the bottom side the structure is Au/Ti/Al/CdTe (rectifying contact). The metallization thickness of the crystal on the top side (irradiation side), measured by the total interference contrast method, is 82 nm. In order to distinguish the sides of the crystal from each other, a 'key' is made on the top side of the crystal (the outermost strip is shortened on one side).

The operating principle of a double-sided strip detector is as follows. The bottom strips are at zero potential, and the top strips are biased with a high voltage of negative polarity. As a result, an almost uniform electric field appears inside the CdTe crystal. At the intersection of the two strips, a virtual elementary SE (pixel) is formed. An X-ray photon interacting with the detector material generates electron-hole pairs. Electrons drift towards the nearest bottom strip, while holes drift towards the nearest top one. As a result, an electric current flows between the two specified strips, integrated by the CSAs connected to them. The amplitude of the signal at the output of the CSA is proportional to the photon energy, and the strip numbers indicate the number of the elementary SE in which the photon interacted with the crystal material. A feature of double-sided strip detectors is that the same signal is measured by two independent processing channels, and since the noise in the channels is uncorrelated, this makes it possible to improve the energy resolution of the detector.

The crystal holder is made of three layers of ADS-96R ceramic. The conductive layer, insulating layers, and high-ohmic resistors are made using thick film technology. The crystal holder ensures that the CdTe crystal is fastened, protecting it from mechanical impacts, and that the conductors to the strips are connected. The crystal holder is mounted through an adapter plate onto a thermoelectric module, which is used to cool the crystal during ground tests. During normal operation of the detector, the crystal temperature is maintained in the operating range by the thermal control system of the ART-XC telescope [12].

Ceramic boards are made of VK-100 ceramics (Polikor, Russia) using thin-film technology. The boards have different metallization topologies and are therefore not interchangeable. VA64TA1 ICs and filter capacitors are installed on the boards. The connection of conductors on the ceramic boards with conductors on the crystal holder and with conductors on flexible printed circuit boards is carried out by wire bonding with gold wire.

Flexible printed circuit boards are hermetically glued into a ceramic case and are used to connect the detector to the control unit. The detector also includes three thermal sensors that control the temperature of the crystal holder and the detector case. Just like the D1 detector, the SD01 detector, after installation into the block, is closed with a hermetic cover with a beryllium window and three-layer shielding.

To process signals from the CdTe crystal, two VA64TA1 ICs (Ideas, Norway) are used [13]. One IC handles signals from the bottom side of the crystal, and the second, from the top side. The IC is manufactured using the 0.35-μm CMOS process (AMS, Austria). The IC die size is 6.985 × 6.020 × 0.725 mm. The channel structure of the VA64TAl IC is the same as in VA32TA IC (see Fig. 4). The VA64TA1 IC is an evolution of the VA32TA IC architecture with reduced power consumption and differs from it as follows:

— the number of signal processing channels is 64;
— the shaping time of the FSH is 300 ns;
— the shaping time of the SSH is from 1.5 to 2.5 us;
— the power consumption of one channel is 0.22 mW;
— the configuration memory size is 360 bits.

The main change to the VA64TA1 IC was the increase in the shaping time to the FSH, which reduced the noise at the FSH output and allowed operation with a lower energy

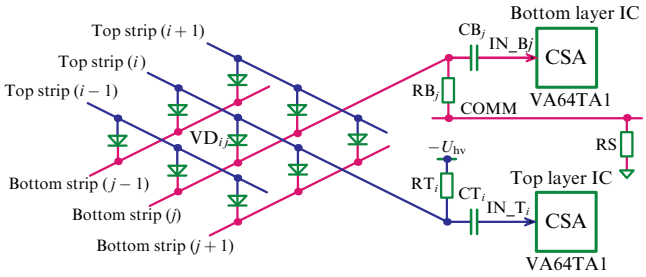

Figure 10. Circuit for connecting SE to inputs of CSA in VA64TA1 IC (i is the strip number on the top side, j is the strip number on the bottom side, VD_{ij} is elementary SE at intersection of strips i and j).

threshold. The connection diagram of an elementary SE to the VA64TA1 IC is shown in Fig. 10. Because the IC can handle both negative and positive input signals, the same type of IC can be used to process signals from the top and bottom strips of a CdTe crystal.

For double-sided strip detectors, it is possible to use a DC connection to the control unit for both the bottom and top strips. However, the use of a DC circuit for the top strips is associated with great technical difficulties, so usually a DC circuit is chosen for the bottom layer and AC for the top layer. In the SD01 detector, we implemented an AC circuit for both the top and bottom layers for the reasons described in the previous section. In addition, the use of an AC circuit for the bottom layer of strips makes it easy to measure the leakage current of a CdTe crystal. For this purpose, all bias resistors RB_j (where j is the number of the bottom strip) are joined up by the 'COMM' signal and connected to the zero potential through the current-measuring resistor RS. The voltage drop across the RS resistor, proportional to the current flowing through the CdTe crystal, is easily measured. Monitoring the crystal leakage current is a very desirable function, because the dependence of the leakage current value on time after high voltage is applied to the crystal allows us to estimate the stability of its electrical characteristics.

The search for a triggered channel (strip) is carried out by an external controller using the same algorithm as for detector D1. Since there are two ICs controlling the detector, to reduce the event processing time, the digitization of signal amplitudes is carried out in parallel by two analog-to-digital converters (ADCs). As a result of the search algorithm, the number of the top strip i and the number of the bottom strip j, in which the maximum signal amplitude is obtained, are determined. The controller servicing the detector stores in the data array the time of the event, the numbers of strips i and j, as well as the signal amplitude in the three bottom strips ($E_{BOT}(j-1)$, $E_{BOT}(j)$, and $E_{BOT}(j+1)$) and in the three top strips ($E_{TOP}(i-1)$, $E_{TOP}(i)$, and $E_{TOP}(i+1)$). Knowledge of the energy release in the region of 3×3 strips makes it possible to classify events as single, double, or triple and to correctly restore photon energy in the case of charge share between strips.

In addition to the regular data array, the controller can generate an extended data array containing all the signal amplitudes in the bottom and top layers, which allows registering the full energy release in the entire crystal. However, this mode is very expensive in terms of the amount of telemetry generated by the detector and is used only for testing the detector and for carrying out specific research (for example, for registration of charged particles).

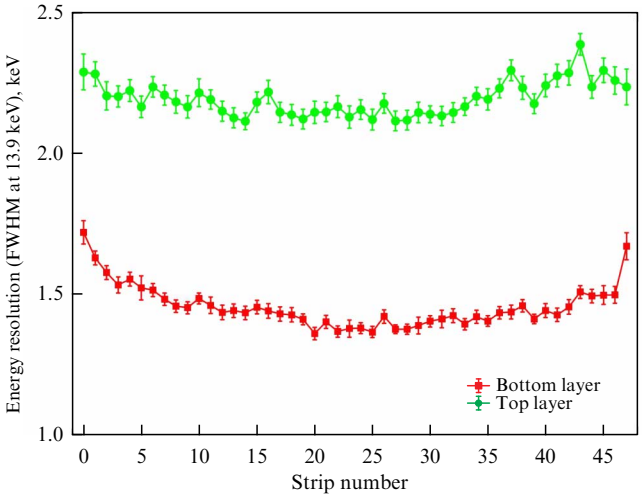

Figure 11. Dependence of energy resolution on the strip number for lower and upper layers of SD01 detector (−20 °C, −100 V).

Calibrations of the SD01 detectors were carried out at the NIKS ground test complex (IKI, Russia) [14] and at the PANTER X-ray test facility (Max Plank Institute for Extraterrestrial physics, Germany). A typical dependence of the energy resolution versus the strip number for the bottom and top layers is shown in Fig. 11. To calculate that dependence, spectra of the ^{241}Am source were used with the selection of only single (in the bottom or top layer) events. The degradation in energy resolution from the central to the peripheral strips is associated with a gradually increasing conductor length between the input of the CSA and the strip and, accordingly, an increasing parasitic capacitance at the input of the CSA. The difference in energy resolution between the bottom and top layers is associated with two factors. The first is the presence of additional leakage current from capacitors operating in the top layer at high voltage, which leads to an increase in electronic noise. The second factor is due to the fact that in CdTe the product of the mobility and lifetime of holes is two orders of magnitude less than that of electrons. Therefore, the peaks in the spectrum collected in the top layer, working with the hole component of the induced signal, broaden towards low energies. Another effect that worsens the energy resolution in the last strips is that, for them, half of the double events occur at the boundary of the strip with the guard ring, and these events are classified as single, which also leads to broadening of the peaks towards low energies.

The efficiency of photon registration by the crystal of the SD01 detector is the same as that of the D1 detector (see Fig. 7).

Seven SD01 detectors as part of the ART-XC telescope named after M N Pavlinsky on the Spektr-RG spacecraft were launched on July 13, 2019 by a Proton-M rocket with a DM-03 booster to the Lagrange libration point L2 of the Earth–Sun system. On July 18, 2019, calibration of the detectors began, and on August 25, 2019, the telescope started observing celestial bodies in regular mode.

To monitor the parameters of the SD01 detectors in flight, they are periodically (approximately once every two months) calibrated using ^{55}Fe and ^{241}Am combined gauge radiation sources. Typical calibration time is one hour. Only one detector is calibrated per day, while the other six continue to survey the sky. This is done so as not to interrupt the

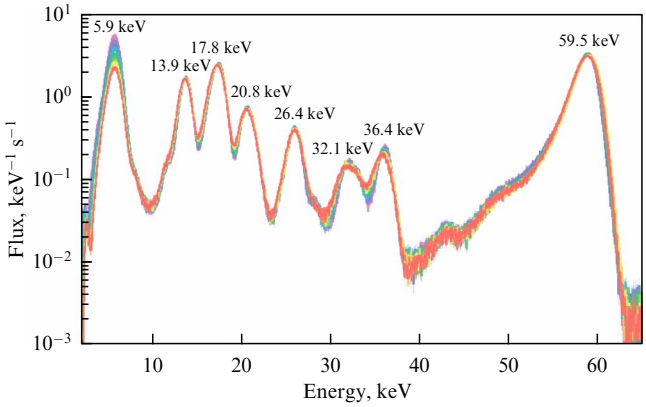

Figure 12. Spectra of a combined calibration source of ^{55}Fe and ^{241}Am collected by SD01 detector for period from December 2019 (purple) to September 2023 (red).

telescope's observation program during calibration. The calibration of all detectors takes seven days. The ADC units-to-energy transfer function for each strip is determined using the calibration data and subsequently used to process the observation data for the period until the next calibration.

Figure 12 shows all spectra of the combined calibration source collected with one detector from December 2019 to September 2023. Each spectrum is the sum of spectra over all elementary SEs (pixels), and to determine the energy of each photon, the energy values registered in the top and bottom layers are added with minimization of the dispersion. The decrease in peak height at 5.89 keV is due to the decay of the ^{55}Fe isotope (half-life is 2.737 years). A slight decrease in the height of the remaining peaks is associated with a gradual degradation in energy resolution due to radiation damage of the CdTe crystal. Currently, all SD01 detectors demonstrate high stability of their parameters.

4. Detector for the Gamma-400 project

Silicon detectors are superior to CdTe detectors in energy resolution due to lower electron-hole pair formation energy, better carrier mobility and lifetime characteristics, more advanced crystals, and better established manufacturing technology. Modern silicon detectors with SDD (Silicon Drift Detector), CCD (Charge Coupled Device), and DepFET (Depleted Field Effect Transistor) structures have come close to the theoretical limit of energy resolution of a silicon detector of 118 eV (FWHM at an energy of 5.89 keV).

Silicon drift detectors (SDDs) [15] have excellent energy and time resolution, but require a separate signal processing channel for each image pixel. This makes SDDs difficult to use as focal detectors with high spatial resolution, but they find application in spectrometers without spatial resolution within the field of view, as in the NICER [16] and LOFT [17] projects, for example.

CCD-based detectors are widely used in X-ray astrophysical telescopes aboard the Chandra, XMM/Newton, Swift (XRT telescope), and Spektr-RG (eRosita telescope) observatories, etc. X-ray CCD chips have proven to be highly reliable products for space applications. For example, the detectors of the eRosita telescope [18] are built on pnCCD with a matrix of 384 × 384 pixels with a size of 75 μm and have an energy resolution of 128 eV (FWHM at an energy of 5.89 keV). Their main disadvantage is the long processing

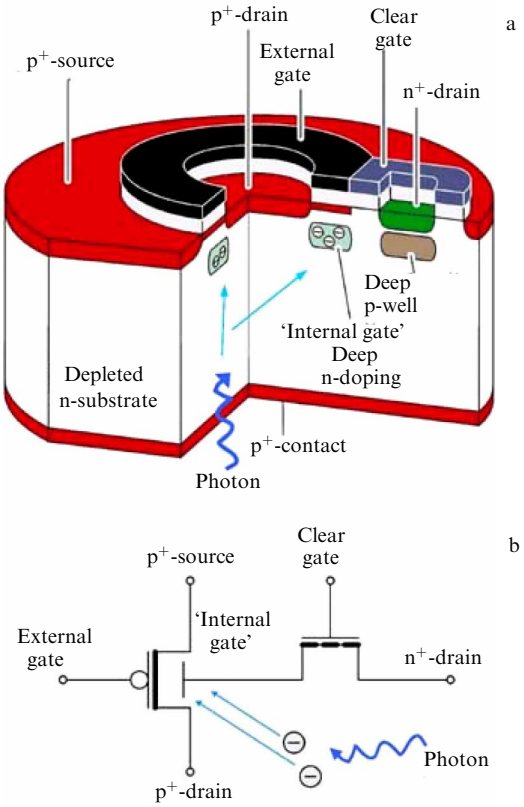

Figure 13. (a) DepFET SE model and (b) its equivalent electrical circuit.

time for one frame (about 50 ms). These detectors are difficult to use for observing bright or rapidly changing sources due to the pile-up effect when operating in full-frame mode. Compared to CCDs, detectors based on DepFET semiconductor structures can provide two orders of magnitude faster performance with the same matrix size and the same energy resolution. For this reason, a DepFET-based detector was chosen for the WFI instrument [19] on the new Athena X-ray telescope (European Space Agency).

The DepFET semiconductor structure [20] operates in the sideward depletion mode. The structure of the DepFET SE and its equivalent circuit are shown in Fig. 13. DepFET is fabricated on a high-resistivity n-type silicon substrate, with p$^+$-contacts formed on both sides of the substrate, forming p–n-junctions to the n-substrate. An additional n$^+$-region is located outside the DepFET SE and provides ohmic contact to the n-substrate. The potentials at the n$^+$-contact and two p$^+$-contacts reverse-biases the p–n-junctions and the regions of their internal space charge overlap, providing depletion across the entire thickness of the substrate (i.e., a positive voltage is applied to n$^+$, and a negative voltage is applied to p$^+$).

If the same negative potential is applied to the p$^+$-contacts relative to the n$^+$-contact, then the maximum potential will be exactly in the middle of the substrate. If a more negative voltage is applied to the bottom p$^+$-contact than to the top p$^+$-contact, then the geometric position of the maximum potential will shift towards the top side of the substrate, simultaneously decreasing in value relative to the potential of the n$^+$-contact. To compensate for this negative effect, additional deep n-type doping is introduced. The presence of additional doping makes it possible to increase the potential in this region almost to the value of the n$^+$-contact potential.

By changing the distribution of the donor dopant, it is possible to control the position (in plane and depth) of this potential maximum, which creates a potential well for electrons in the substrate. Thus, all free electrons produced due to thermal generation or absorption of a photon will drift towards the potential well and remain there until they recombine. All free holes that appear will drift in the direction of the p^+-contacts.

The lower p^+-contact is made very thin because it is the entrance window of the SE for registered photons. The upper p^+-contact, separated by a polysilicon gate (external gate), forms a p-channel MOSFET. Applying a negative potential to the external gate relative to the p^+-drain forms a p-channel under the gate and provides a flow of current between the drain and the source of the transistor. However, the accumulation of electrons in the potential well under the channel of the MOS transistor with the appearance of a negative potential relative to the potential of the p^+-source leads to the same result, i.e., channel formation and current flow between source and drain. The deep n-doping region is called the 'internal gate' because of its ability to modulate the transistor's channel conductance. Let us assume that at the initial moment of time there are no electrons in the potential well and constant voltages are applied to the electrodes of the transistor. This provides a constant drain current flow. As the potential well is filled with electrons, the drain current will begin to increase, and the increase in drain current will be proportional to the number of electrons entering the potential well. The number of stored electrons can be determined by measuring the change in the drain current.

The channel width will increase and reach a maximum as electrons accumulate in the potential well, after which the arrival of additional electrons will no longer modulate the conductivity of the channel and the structure will lose its amplifying properties. The DepFET has a second built-in MOSFET, called a reset transistor, to remove electrons from the potential well. A p-well is formed to create this transistor and isolate it from the main transistor of the structure. The reset transistor is an n-channel MOSFET and consists of an n^+-drain, a polysilicon gate, and a deep n-doping region (source). The charge can be completely removed from the internal gate and the amplifying properties can be returned to the structure by applying a positive potential to the n^+-drain and the gate of the reset transistor.

The DepFET SE has a number of remarkable properties that make it an 'ideal' structure for detecting X-ray photons:

— simultaneous signal generation and amplification without intermediate contacts;

— ultra-low capacitance of the internal gate at the level of femtofarads;

— the possibility of long-term storage of accumulated electrons;

— the possibility of multiple, nondestructive measurements of the accumulated charge;

— good efficiency at low energies due to a very thin and uniform entrance window;

— the ability to form SE matrices without boundaries between them;

— the ability to detect radiation when the main transistor and reset transistor are closed.

The dimensions of the main MOS transistor tend to be made as small as possible to reduce the value of the internal gate capacitance and obtain maximum gain, but at the same time the size of the SE is reduced. In order to make the size of the SE larger than the size of the main MOS transistor, it is necessary to ensure the drift of electrons into the potential well not only in the vertical, but also in the horizontal direction. This is achieved by creating a system of concentric electrodes (rings) around the MOS transistor on the top (device) side of the substrate. By applying a certain potential distribution to these rings, it is possible to generate an electric field in the horizontal direction so that all electrons move towards the inner gate. The result is a hybrid of SDD and DepFET structures. For structures 100 μm in diameter, one drift ring is used, for 150 μm, two, etc.

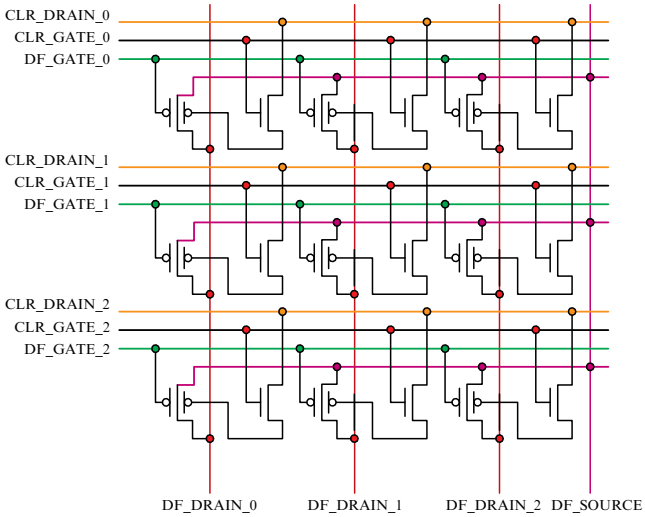

Figure 14. Electrical circuit of a 3 × 3 DepFET SE matrix.

The ability to accumulate a charge when both SE transistors are in the off state allows organizing the DepFET SEs into a two-dimensional matrix, thereby greatly reducing the required number of external signal processing channels. The electrical circuit of a matrix with a size of 3 × 3 DepFET SEs is shown in Fig. 14. The same constant voltage is applied to the sources of all transistors in the matrix (signal 'DF_SOURCE'). The column wires ('DF_DRAIN' signals) are connected to amplifiers. Work with the matrix is carried out row by row, with each row controlled by three signals. The 'DF_GATE' signal turns on the main transistors of the SEs in a single row. Since the transistors in all other rows are turned off, the drain of only one transistor is connected to each column wire, which allows measuring its current and determining the amount of charge accumulated on the internal gate. This is the so-called first sample. Next, the reset transistor is turned on (with the signals 'CLR_DRAIN' and 'CLR_GATE'), and the accumulated charge is removed from the internal gate. Then, the drain current is measured again in the absence of accumulated charge, i.e., a second sampling is done. Based on the difference between the values of the first and second samples, the number of accumulated electrons and the energy of the registered photon are estimated. After processing the current row, all transistors in this row are switched off and this algorithm is repeated for the next row. This method of polling the matrix is called the 'rotating shutter' method.

Two types of ICs are required to control the DepFET SEs matrix. The first one is called a 'switcher.' The purpose of this IC is to apply control signals to the rows of the matrix to select the active row and reset the DepFET elements. A typical IC of this type is the Switcher-A [21] for the WFI instrument. The

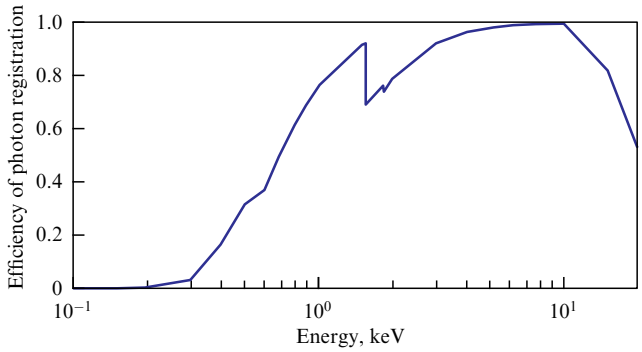

Figure 15. Photon detection efficiency with a 725-μm-thick silicon detector (external filter: Al (100 nm) and mylar (300 nm); optical filter on the die: Al (200 nm), Si_3N_4 (40 nm), and SiO_2 (30 nm)).

second type of IC is multi-channel time-variant amplifier-shapers. The CAMEX series ICs [22] belong to this type. CAMEX ICs are designed to work with both CCD-based detectors (for example, CAMEX 128JD IC, used in the eRosita telescope [23]) and DepFET-based (for example, CAMEX PIXEL 64L).

The reading time for one frame is equal to the row processing time multiplied by the number of rows. The following methods are used to reduce readout time and increase detector performance. The frame is divided into two half-frames, and each half-frame is processed by its own set of ICs in parallel, which doubles the readout speed. The second method is to process two rows at a time instead of one row, which also doubles the read speed and also requires doubling the number of signal processing channels. Using both methods simultaneously, the frame reading time can be reduced fourfold, but the speedup will have to be paid for by quadrupling the number of signal processing channels and almost quadrupling the power consumed by the detector.

In the preliminary design of Gamma-400, IKI proposed the use of a detector based on a matrix of DepFET elements as a focal detector for a telescope with X-ray optics similar to the optics of the ART-XC telescope named after M N Pavlinsky. General parameters of the detector:

— matrix size is 192 × 192 SEs;
— SE diameter is 150 μm;
— die thickness is 725 μm;
— linear size of the sensitive area is 28.8 × 28.8 mm;
— energy resolution is 150 eV (FWHM at an energy of 5.89 keV);
— dynamic range is 20 keV;
— frame reading time is 432 μs (when reading two rows simultaneously);
— power consumption by the detector is 5 W;
— die operating temperature is from −100 to −80 °C.

PNSensor (Germany) was planned to be the manufacturer of the DepFET SEs matrix and the control and signal processing ICs.

The calculated efficiency of photon registration by a silicon detector with a thickness of 725 μm is shown in Fig. 15. This curve takes into account the presence of an external protective window in front of the die and an optical blocking filter on the surface of the die. The protective window consists of Al (100 nm) and mylar (300 nm). The optical filter on the die consists of three layers: Al (200 nm), Si_3N_4 (40 nm), and SiO_2 (30 nm).

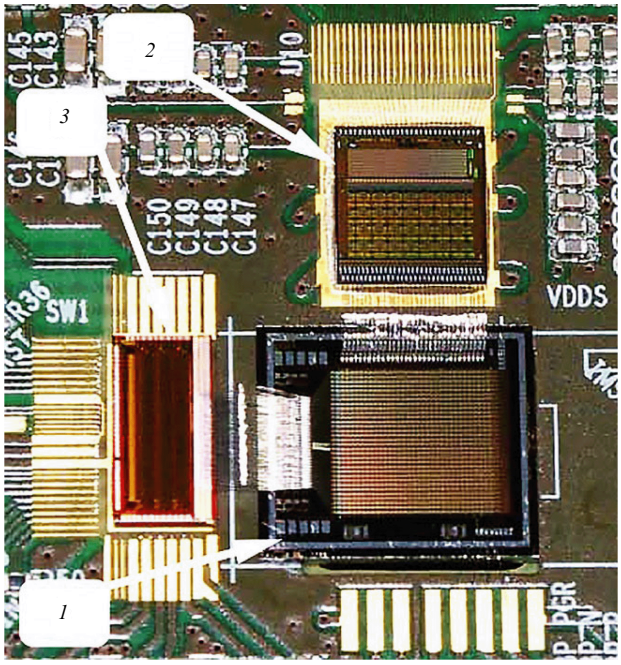

Figure 16. Prototype detector (PNSensor, Germany): *1* — 32 × 32 DepFET SE matrix; *2* — CAMEX PIXEL 64L IS; *3* — SWP1 IS.

As part of a preliminary design commissioned by IKI, PNSensor manufactured a prototype detector with a 32 × 32 DepFET SE matrix 150 μm in size. The prototype detector is shown in Fig. 16. The model includes a DepFET SEs matrix, an SWPl IC (64-channel switcher), and a CAMEX PIXEL 64L IC (64-channel amplifier-shaper). The DepFET SEs matrix in the prototype detector ensures the reading of two rows simultaneously, thereby accurately simulating the operating algorithm of a full-sized detector.

The control unit and hermetic container for testing the detector were designed and manufactured by IKI. The manufactured equipment is shown in Fig. 17. Tests were carried out in a climate chamber. During testing, the detector prototype was placed in a hermetic container, which was filled with dry nitrogen with a dew point below −45 °C.

A combined ^{55}Fe and ^{241}Am radiation source was used to calibrate the detector. The entire data stream (i.e., full frames of 32 × 32 SEs) was recorded on the hard drive of a personal computer for subsequent processing. Processing of the accumulated data was carried out after the completion of observations (post facto). The processing algorithm is as follows. In the first phase, using all received frames for each SE (pixel), a raw amplitude spectrum was plotted. In the raw spectrum, the positions of peaks with known energy were identified, and the resulting points on the 'energy versus ADC units' curve were approximated by a quadratic function. The result was 32 × 32 functions for the conversion from ADC units to energy. In the second phase, all accumulated frames were converted from ADC units to energy units. In the third phase, the following operations were performed for the first frame:

— searching for a pixel in which the signal amplitude exceeded the specified threshold value (in energy units);
— saving a cluster of 3 × 3 pixels around the found pixel.

After finding all the clusters within the frame that were candidates for the event, intersections between clusters were searched for and two (or more) intersecting clusters were combined into one. Next, an event classification operation

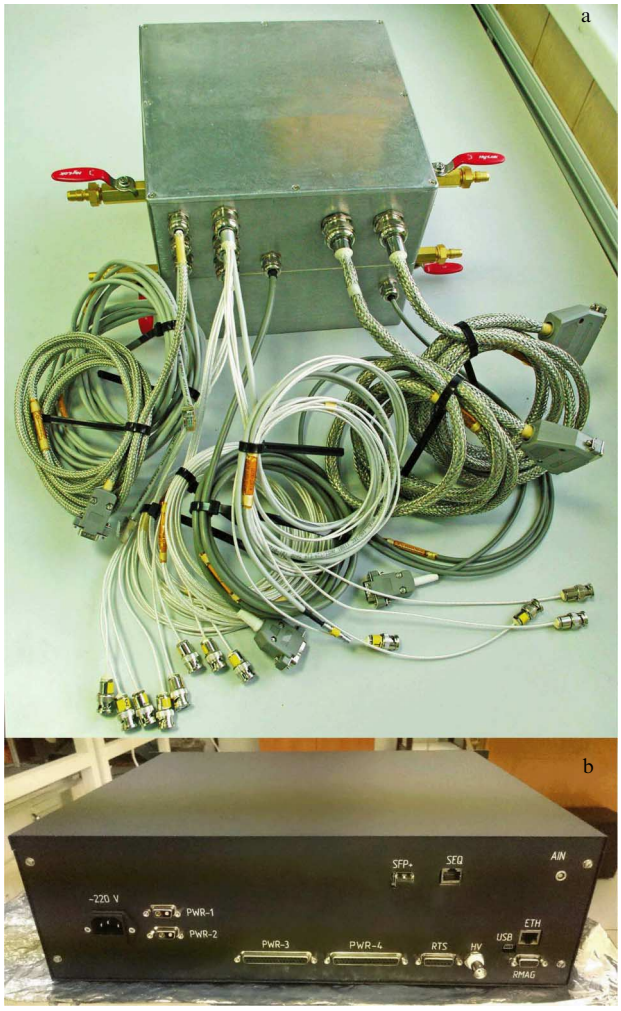

Figure 17. (a) Hermetic container for the detector and (b) detector control unit.

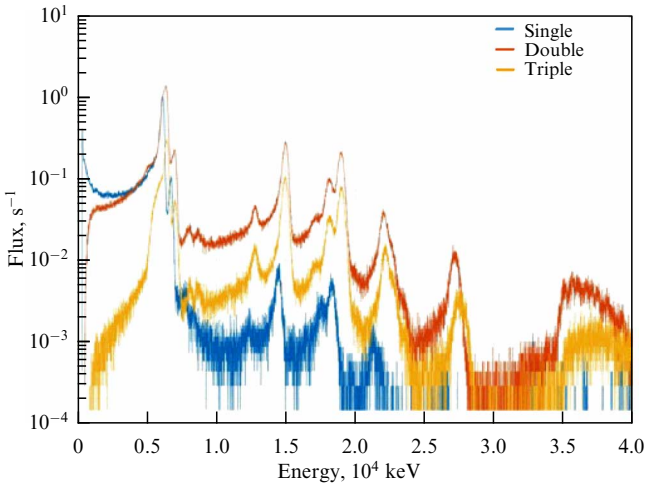

Figure 18. Spectra of a combined X-ray source of ^{55}Fe and ^{241}Am (spectra of single, double, and triple events are shown separately) (−41 °C, −400 V).

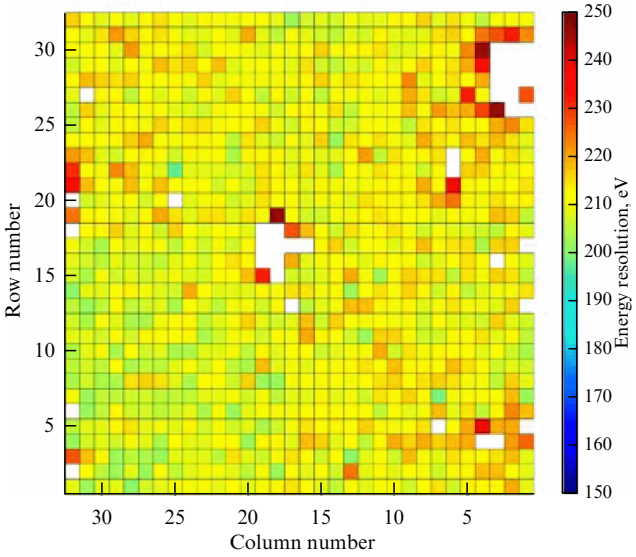

Figure 19. Distribution of energy resolution over detector pixels (FWHM at an energy of 5.89 keV) (−41 °C, −400 V).

was carried out for each cluster. An event is considered 'single' if, within the entire cluster, the signal amplitude in only one pixel was above the threshold, and the photon energy is considered equal to the energy registered in this pixel. An event is considered 'double' if the amplitude above the threshold is registered in only two adjacent pixels within the cluster. Then the photon energy is calculated as the sum of the amplitudes in two pixels. The photon registration coordinate is considered to be the pixel number with the larger amplitude. An event is considered 'triple' if the signal amplitude in three adjacent pixels located in the letter 'L' exceeds the threshold. The photon energy is now calculated as the sum of the amplitudes in three pixels. The photon registration coordinate is also considered to be the number of the pixel with the larger amplitude. Clusters with other energy release configurations were not used to create the spectra of the calibration source, since, in our opinion, they cannot be generated by photons in the working energy range. For each event, from all those found within the frame, a data array was formed containing frame time, pixel number, photon energy, and event type. Next, all collected frames were processed using this algorithm. In the fourth phase, using the obtained data arrays of events, three amplitude spectra (of single, double, and triple events) were created for each pixel. The result of summing all spectra over all detector pixels as a result of this algorithm is shown in Fig. 18.

An obvious problem with these spectra is the shift in the position of the maxima of the same peaks relative to each other, so they cannot simply be added to obtain the final spectrum. Therefore, this result should also be considered to be intermediate. The next iteration is necessary to determine for each pixel three new energy-unit-to-energy-unit transfer functions, bringing the spectra of single, double, and triple events to a single energy scale. After this, it is possible to obtain the final spectrum. An evaluation of the detector energy resolution is shown in Fig. 19. Pixels in which the noise level exceeds 250 eV are colored in white. The area-averaged energy resolution of the detector was 211 eV (FWHM at an energy of 5.89 keV). For the flight detector, the goal is to obtain an energy resolution of no more than 150 eV.

The huge generated data stream is the main difficulty in working with DepFET-based detectors. For a detector with 192 × 192 pixels and a frame capturing time of 432 μs and digitizing two bytes per pixel, the 'raw' data flow will be 170.7 MB s^{-1}. Obviously, it is impossible to store such a volume of data in an on-board computer and transmit it to

Earth. In addition, the speed of currently existing microprocessors approved for use in space is clearly insufficient to solve the problem of searching for events in this data stream in real time. From our point of view, the only solution to this problem is the following. In the first phase, a specialized hardware controller performs searches for 3×3-pixel clusters in the event stream, thereby significantly reducing the data stream. In the second phase, the found clusters are transferred for processing to a high-speed digital signal processor, whose task is to classify events, select single, double, and triple events from them, and reject events of other types, obviously not related to photons of the working energy range. In the third phase, data arrays of single, double, and triple events are transferred to a general purpose processing unit that performs tasks of packaging received data into telemetry frames and storing and transmitting them to a radio data link.

As part of the preliminary design, a special hardware controller was designed and its feasibility on field-programmable gate array ICs was assessed.

The preliminary design received approval in 2019, however, as of the time of writing this article, the development work on the Gamma-400 project had not moved to the next stage.

5. Conclusion

In recent years, a number of semiconductor X-ray detectors for astrophysical instruments have been designed and manufactured at the Space Research Institute (IKI). SD01 detectors have undergone flight tests and are being operated on Spektr-RG spacecraft as part of the ART-XC telescope named after M.N. Pavlinsky. The D1 detectors are planned for launch in 2024 as part of the MVN space payload. Currently, the IKI is designing promising silicon detectors for future missions. An additional area of work is to develop our own ICs for processing signals from semiconductor detectors and expand the list of potential contractors with experience and the ability to manufacture sensitive elements.

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