Physics – Uspekhi **62** (8) 754 – 794 (2019)

REVIEWS OF TOPICAL PROBLEMS

PACS numbers: 81.05.ue, **81.10. – h**, **85.30. – z**

SiC-based electronics

(100th anniversary of the Ioffe Institute)

A A Lebedev, P A Ivanov, M E Levinshtein, E N Mokhov,
S S Nagalyuk, A N Anisimov, P G Baranov

DOI: https://doi.org/10.3367/UFNe.2018.10.038437

Contents

Abstract. We review the history and modern state of silicon carbide and SiC-based devices. The main techniques for growing bulk SiC crystals and epitaxial SiC films are discussed. Epitaxial SiC structures used for post-growth processing are briefly reviewed. The state of the art achieved in developing SiC devices is presented. The main problems that occur in developing SiC equipment and prospects for designing and developing such equipment are analyzed.

Keywords: silicon carbide, bulk crystal, sublimation, polytype, lateral overgrowth, dislocation, high-voltage power diode, high-voltage subnanosecond pulse diode, thyristor, bipolar junction transistor, analytic model, computer simulation, color center, spin, sensorics, magnetic field, ODMR, graphene, two-dimensional material, Raman spectroscopy

A A Lebedev (*), **P A Ivanov, M E Levinshtein, E N Mokhov, S S Nagalyuk, A N Anisimov, P G Baranov** (†)
Ioffe Institute, ul. Politekhnicheskaya 26, 194021 Saint Petersburg, Russian Federation
E-mail: (*) shura.lebe@mail.ioffe.ru, (†) pavel.baranov@mail.ioffe.ru

Received 4 September 2018, revised 1 October 2018
Uspekhi Fizicheskikh Nauk **189** (8) 803 – 848 (2019)
DOI: https://doi.org/10.3367/UFNr.2018.10.038437
Translated by M Zh Shmatikov; edited by A M Semikhatov

1. Introduction

We here review the work on developing electronics based on silicon carbide, a significant part of which has been done at the Ioffe Physical-Technical Institute (Ioffe Institute). Section 2 contains a brief analysis of electrophysical properties of SiC and other broadband semiconductors from the perspective of engineering various types of devices. Section 3 presents a description of the methods designed to grow bulk high-quality silicon-carbide crystals up to about 0.1 m in diameter, both pure and doped, and enriched in their own isotopes. Options for controlled growth of various silicon-carbide polytypes are presented. Lateral overgrowth of seed crystals is shown to enable a significant decrease in the density of edge dislocations located perpendicular to a foil surface.

Section 4 contains experimental data on the development and studies of high-voltage (1–3 kV) 4H-SiC diodes for power and short-pulse electronics. Power diodes containing an integrated Schottky p – n structure (junction barrier Schottky, JBS) combine small reverse recovery times and low losses under switching. Fast-recovery avalanche p – n diodes feature reverse recovery times comparable to those of JBS diodes and can scatter an energy of several J cm^{-2} in the avalanche current pulse mode. 4H-SiC diode circuit breakers — fast-recovery drift diodes — generate high-voltage pulses whose pulse leading edge is in the subnanosecond time range.

In Section 5, we use analytic models and computer simulations with the original 'Issledovanie' (Research) soft-

ware package to explore the main processes that occur in power bipolar 4H-SiC-based devices, including thyristors, bipolar transistors, and diodes. We also consider phenomena common to all silicon-carbide-based bipolar devices: electron–hole scattering, the efficient emitter problem, and fundamental physical restrictions on the maximum blocked voltage and maximum current densities. Unique quantum properties of color centers in silicon carbide enable establishing a new role for silicon carbide as a flexible and practical platform for developing modern quantum technologies. Atomic-size color centers in bulk and nanocrystal SiC are promising systems for spintronics, photonics compatible with the passband of fiber optics and living systems, quantum information processing, and environmental sensing. The options provided by high-temperature optical spin manipulations with both spin ensembles and individual spins have opened a new era in the use of spin phenomena in both fundamental science and applied research.

In Section 6, we consider a technology for obtaining graphene films by the method of thermal destruction of the surface of SiC single crystals. These films, which are shown to exhibit high structural perfection, can be used to engineer supersensitive gas sensors and biosensors.

In the concluding Section 7, we present the main results of and prospects for the development of SiC electronics.

2. Electrophysical properties of silicon carbide

Modern civilization needs increasingly efficient power sources to maintain humankind's progress. Nuclear power and conversion of solar radiation using ground-based and orbital facilities will arguably become the main power sources of the future. Today's power electronics that use silicon-based devices are gradually losing their ability to meet ever growing requirements for functionalities, mass, volume, operation resource, and reliability of converters. Semiconductors with a large bond energy, such as diamond, GaN, and SiC, are traditionally regarded as possible replacements for silicon in manufacturing power semiconductor devices.

Advancements in technology that have been witnessed during the last 10 to 15 years have enabled engineering SiC-based devices in which the expected high capacities of SiC with regard to switching power and high operation temperatures have been implemented. SiC is widely used in optoelectronics as a substrate for LEDs emitting in the visible range and as a material to manufacture power diodes and transistors operable under extreme conditions: high temperatures, hard-radiation effects, and electric and magnetic fields. Special attention has been paid lately to prospects of using SiC to engineer quantum amplifiers (masers). Of great interest are also sources of individual photons based on silicon vacancies in SiC that operate at room temperature in the infrared range, a capacity that is of special importance for medical applications.

We only review the areas of SiC electronics that are the most promising ones in our opinion. We note that a significant and sometimes decisive contribution to these areas has been made by the Ioffe Institute's researchers.

2.1 Development of technology for producing silicon carbide and devices based on it: a history

Berzelius was the first to discover a chemical compound consisting of silicon and carbon (1824). C M Despretz obtained this compound in 1849 by reducing silica with carbon. H Moissan independently discovered SiC crystals in studying meteorites in Diablo Canyon in the Arizona desert. In 1905, this mineral was named 'moissonite' to commemorate its discoverer. This name is currently used for jewelry made of silicon carbide. In the late 20th century, Acheson developed and patented a method to manufacture SiC on an industrial scale [1]. The crystals grown using this method are heavily doped (up to 10^{21} cm^{-3}), lack polytype uniformity, and have small dimensions, $10 \times 10 \times 3$ mm^3 [2].

In studying such specimens, Round in 1907 observed luminescence that emerged when electric current was flowing through a crystal [3]. Losev studied silicon-carbide luminescence in more detail in 1923–1940 [4]. He found that one of the luminescence types is related to the presence of a special 'active layer' on the crystal surface. Losev showed later that this layer exhibits electron conductivity, while the specimen volume exhibits hole conductivity. He also found that rectification and electroluminescence are interrelated. The two phenomena of utmost importance for semiconductor electronics — electroluminescence and rectifying properties of p–n structures — were thus identified for the first time in SiC crystals. Because the electronics industry was manufacturing vacuum electric bulbs at that time, these discoveries unfortunately remained unnoticed.

Commercial interest in semiconductors is known to have emerged after W Shockley discovered the transistor effect in Ge crystals in 1949. At about the same time, Lily, a Dutch physicist, proposed a new method to obtain SiC crystals [5]. Single crystals are produced with this method by subliming SiC through a vapor phase from hotter areas to cooler ones. Sublimation is performed in an inert environment (argon) at a temperature of 2500–2650 °C. This method enables the production of crystals whose surface area is up to 4 cm^2 and density of uncompensated impurity is $10^{16}-10^{19}$ cm^{-3}. The method has several disadvantages: high growth temperatures and uncontrollable nucleation and growth of crystals.

Searches began in the first half of the 1950s for semiconductor materials that can operate at higher ambient temperatures than Ge. Many researchers were attracted to silicon and silicon carbide. Numerous studies where the properties of SiC were explored and semiconductor devices based on it were developed have been performed over the next 10–15 years.

However, by the early 1970s, commercial interest in silicon carbide had faded again. This was apparently due to accomplishments in the development of Si and GaAs technologies that were incomparably more successful than those in SiC technology. Due to significant technological problems encountered in growing silicon carbide and developing devices on its basis, the actual parameters of these devices were much inferior to the expected ones. Several research teams, most of which worked in the USSR, continued studies of SiC properties throughout the next 15 years.

A sublimation 'sandwich method' to grow epitaxial SiC layers was proposed in 1970 at the Ioffe Institute [6]. The essence of the method is that growth occurs in the process of a vapor source and substrate coming closer to each other. Epitaxy was performed in a vacuum, owing to which the process temperature was reduced to 1810–1910 °C.

A technique to grow bulk SiC crystals [7], a modified Lily method, was proposed in the late 1970s. This method is based on vapor condensation onto a single-crystal substrate. Growth occurred at a temperature of about 2000 °C. The diameter of the grown ingot is determined by the substrate size (currently, up to 150 mm) [8].

Interest in silicon carbide as a promising material for semiconductor electronics was rekindled after S Nishino had developed the chemical vapor deposition (CVD) method for epitaxy of 3C-SiC films onto silicon substrates [9]. The use of standard production facilities and large-area substrates provided new options for rapid commercial implementation of the results obtained. Field-effect transistors of several types based on such films were created shortly afterwards [10]. The electrophysical properties of this material have been studied in detail [11]. However, both the parameters of the devices and the quality of films themselves remained not quite satisfactory. Apart from this, 3C-SiC is the most narrow-band compound among silicon-carbide polytypes (with the bandgap width $E_g = 2.4$ eV) and is only insignificantly superior to GaP with regard to maximum operation temperatures. The same CVD method was briefly used to obtain 6H-SiC films based on 6H-SiC substrates [12]. Owing to this, semiconductor devices of virtually all types have been engineered based on silicon carbide: LEDs emitting in the blue spectrum range, ultraviolet (UV) receivers, Schottky diodes, rectifying diodes, field-effect transistors, bipolar transistors, and thyristors [13].

2.2 SiC parameters of importance for electronics

Two areas are rapidly developing in the modern physics of superconductors: (1) properties of materials are being modified by changing the geometric dimensions of structures (the physics of nanostructures) and (2) new semiconductor materials are being developed and explored. Of importance for the second area are studies of broadband semiconductors. Options for broadband materials for engineering semiconductor devices were analyzed long ago [14–16]. Because their bandgap width is larger than that of Si and GaAs, broadband materials have the following advantages:

- higher operation temperature;
- the possibility of creating, based on these materials, light-emitting devices that radiate in the visible range;
- high critical breakdown fields (E_{cr});
- high radiation resistance.

Table 1 displays the main characteristics of some semiconductor materials, including their Debye temperature T_D, which is known to be expressible in terms of the maximum energy of the phonon E_{ph} that exists in a given material as

$$T_D = \frac{E_{ph}}{k_B},$$

where k_B is the Boltzmann constant. If the temperature exceeds T_D, lattice oscillations become inelastic, resulting in decomposition of the material. This decomposition can occur in various semiconductors due to the growth of dislocations, decomposition of binary compounds, etc. The temperature T_D can thus be regarded as a characteristic of the upper temperature level for operations of devices based on this specific material. We note that T_D of GaN is lower than that of SiC. There is also an entire class of broadband materials (II–VI) whose T_D is even lower than that of GaN. This helps explain why all the attempts that have been made to date to engineer high-power high-temperature devices based on compounds II–VI have failed, despite their broader energy gap. It is also indicated in Table 1 whether each material is a semiconductor with a direct or indirect bandgap structure and whether a substrate of a large diameter made of the same material is available (+) or not (–). The first factor essentially determines whether the material can be used for optoelectronic devices; the second sets prospects for implementing academic results in commercial production.

Table 1. Characteristics of some semiconductor materials.

Characteristic	Si	GaAs	4H-SiC	GaN	Diamond
E_g, eV	1.12	1.43	3.26	3.39	5.45
Direct band structure		+		+	
Critical strength of breakdown field, MV cm^{-1}	0.3	0.6	3	> 3	10
Thermal conductivity, W cm^{-1} K^{-1}	1.5	0.46	4.9	1.3	11
Electron mobility, cm^2 V^{-1} s^{-1}	1500	8500	800	1250	2200
Availability of its own substrate	+	+	+	– 600	– 1850
Debye temperature T_D, K	650	350	1200	2.5	2.7
Saturation rate, 10^7 cm s^{-1}	1	1	2	10	5.7
Dielectric constant ε	11.7	12.9	10		

Table 1 shows that silicon carbide is superior to classical semiconductors, Si and GaAs, in virtually all of the considered criteria. It is of interest to compare this material with other broadband counterparts.

SiC is inferior to GaN in a number of parameters such as low probability of radiative recombination (as in an indirect-bandgap semiconductor). However, there are no substrates for GaN made of the same material, while the substrates for AlN have very small dimensions and are very expensive. GaN is grown by the heteroepitaxy technique using substrates made of other materials (SiC or sapphire). This results in a very high dislocation density in the grown films ($> 10^7$ cm^{-2}). Dislocations in GaN are located perpendicular to the surface of the growing layer and aggregated into clusters. As a result, the growing layer acquires a cellular (grain) structure, which increases the leakage current of p–n structures and causes their degradation with time.

Overall, SiC is a material that is more promising for engineering power devices than GaN and other nitrides (III–N) are. The lifetime of charge carriers in GaN, which cannot in principle be large (due to a high probability of radiative recombination), limits the use of this material for engineering bipolar junction devices. The maximum dissipated power is reduced in unipolar devices due to low thermal conductivity and a lower Debye temperature. Other electrophysical parameters (the carrier saturation rate, breakdown field, and mobility) do not provide any significant advantages to bulk GaN over silicon carbide. Nevertheless, GaN Schottky diodes may prove to be competitive with SiC Schottky diodes at voltages up to 1000 V owing to their significantly lower production cost [17].

However, development of heterojunctions in the GaN–AlGaN system enabled the creation of structures containing a 2D electron gas with a significantly higher mobility of carriers. Such structures can be used to engineer high electron mobility transistors (HEMTs) whose parameters are superior to the parameters of field-effect transistors based on bulk SiC. Diamond is unparalleled in both parameters and maximum operation temperatures. However, attempts to obtain single-crystal diamond layers using heteroepitaxy failed, and the substrates made of the same material have a small area and are rather expensive. In addition, there are some problems with obtaining p–n structures in diamond.

A final conclusion can thus be drawn: SiC is currently the most promising material for engineering power devices among the most developed materials and the most developed material among the promising ones.

3. Growing bulk silicon-carbide crystals

To produce semiconductor devices, some manufacturing problems need to be resolved that are related to the production of bulk crystals with high structural perfection [18]. High-quality crystals must be grown with a low level of background impurities; the isotopic composition of crystals must be controllable, and the required polytype must be produced. To manufacture devices, large crystals are needed (dimensions of no less than 150 mm) on whose basis epitaxial structures can be produced in modern reactors.

Bulk SiC crystals are primarily grown by means of physical vapor transport (PVT) through a vapor phase. Commercial crystals are manufactured in the USA, Japan, Germany, and other countries; however, the most successful in this area is US-based Cree Inc. This company has recently grown SiC crystals of 4H and 6H polytypes up to 150 mm in diameter. The problem of micropores (micropipes) has virtually been resolved in recent times, and the density of edge dislocations perpendicular to the surface has been greatly reduced (to 10^2 cm^{-2} [19]).

Semi-insulating SiC crystals are actively grown today. Several methods have been proposed to grow such crystals; they involve adding impurities (V, Co) or intrinsic defects to the crystal to create deep amphoteric-type levels in the bandgap [20]. Significant progress has also been attained in growing pure crystals having a low level of background impurities (less than 10^{16} cm^{-3}) such as nitrogen and boron [21].

Work related to growing semiconductor SiC using the PVT method has been conducted at the Ioffe Institute since the mid-1960s. A sublimation method for growing SiC crystals and epitaxial layers was proposed in 1970; according to this method, which is now referred to as the sublimation sandwich method (SSM) [22], a sublimating source and seed separated by a gap are placed into a temperature field (Fig. 1). To increase the efficiency of mass transport and decrease losses of source vapors, the gap between the source and the seed was set to be rather narrow, no more than 0.2 of the source size.

The method described enables the growth of both epitaxial layers and bulk crystals of SiC [23], as well as other semiconductor materials, for example, GaN [24] and AlN [25]. In the ensuing years, we proposed to use a modification to grow SiC containers made of tantalum [26] rather than graphite, which enables a great increase in the efficiency of mass transport and purity of the crystals and a reduction in losses of the evaporated source.

An unquestionable advantage of the SSM is that it enables growing high-quality crystals in a broad range of temperatures (1600–2600 °C for SiC) under various pressures of inert gas or in a vacuum and in the presence of various dopants. Owing to this, optimal conditions can be created to grow high-quality crystals and control impurities, deviations from stoichiometric composition, and polytypism. The dependence of the SiC crystallization rate on the temperature, the temperature difference, the inert gas pressure, and the distance between the source and seed has been analyzed in detail in [27, 28] in comparing theoretical results with experiment.

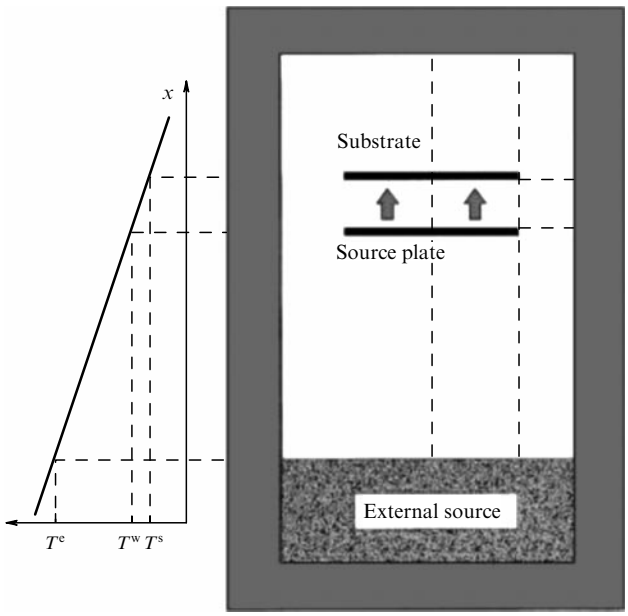

Figure 1. Schematic diagram of a sandwich cell. The left-hand part shows the temperature distribution along the heater axis.

3.1 Growing and characterizing SiC crystals

SiC crystals have been grown in resistance ovens. Polycrystalline SiC sources have been synthesized from semiconductor silicon and spectrally pure carbon. The growth chamber was blown off with an inert gas containing H_2 to reduce strains that emerge due to machining the seed surface.

A general view of the facility for sublimation growth of SiC and AlN crystals up to 6 inches in diameter is shown in Fig. 2. The facility is equipped with a state-of-the-art vacuum system containing a turbomolecular pump, an automated system for monitoring and controlling the growth of crystals, and a system for a separate feed of the main and makeup gases directly into the growth-cell volume. Figure 3 shows polytype-6H SiC crystals 100 mm in diameter grown in this facility. After a crystal has been produced, it is machined and cut into plates. The obtained SiC crystals are virtually colorless (Fig. 3b), which indicates their high purity. The specific resistance of pure crystals is over 10^5 Ω cm.

The density of impurities was measured using secondary ionization mass spectrometry (SIMS). Measured densities of the main impurities are shown in Fig. 4. The concentration of boron and nitrogen in the specimens that were deliberately not doped is at the level of 10^{16} cm^{-3}, while the concentration of Al was at the level of 10^{15} cm^{-3}.

Figure 5 shows a map of how specific resistance is distributed in polytype 6H undoped SiC specimens. We note that high resistance was attained in these specimens without adding dopants or defects that create deep levels in the bandgap.

3.1.1 Growing crystals of a specific isotopic composition. Silicon-carbide crystals with a modified isotopic composition have been grown using the ^{28}Si isotope: preprocessed silicon was used in the form of small lumps (1–3 mm) whose isotopic composition is 99.999% ^{28}Si. The ^{28}Si isotope is stable. The source for growing silicon-carbide crystals with the modified isotopic composition was synthesized similarly to the source with a natural content of isotopes. The crucible and internal fitting of the oven were degassed prior to the

Figure 2. Facility for growing SiC crystals up to 6 inches in diameter.

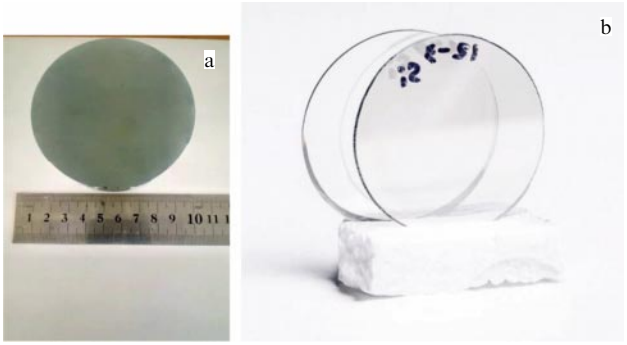

Figure 3. Images of a polytype-6H SiC plate (a) doped with nitrogen and (b) without impurities. The plates are 100 mm in diameter. We can see that the undoped plate is virtually colorless (to stress this feature, the colorless plate is especially marked in black).

synthesis procedure at a temperature of 2200 °C and under a vacuum of 10^{-5} Torr for 3 hours in a resistive heating facility, after which a stoichiometric composition mixture of powder carbon and silicon (^{28}Si) was uploaded into the crucible. Silicon carbide powder was prepared. A polytype-6H silicon-carbide plate with (0001) orientation about 15 mm in diameter was used as a seed crystal. After the ^{28}SiC silicon-carbide crystal had been grown, it was machined and cut into plates. The density of impurities and isotopic composition were measured using the SIMS method. The measured densities of the main impurities are presented in Fig. 6. The data displayed show that the ^{28}Si isotope content is at a level of 99.799%, while the natural content of this isotope is about 92.255%. A low concentration of aluminum, 1.6×10^{14} cm^{-3},

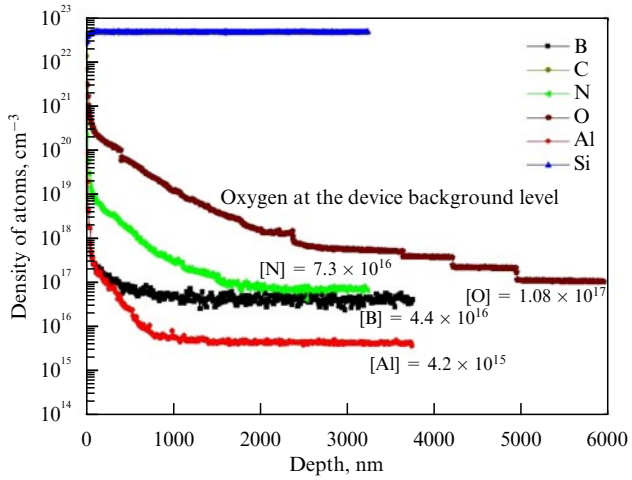

Figure 4. (Color online.) Density of background impurities in undoped SiC crystals.

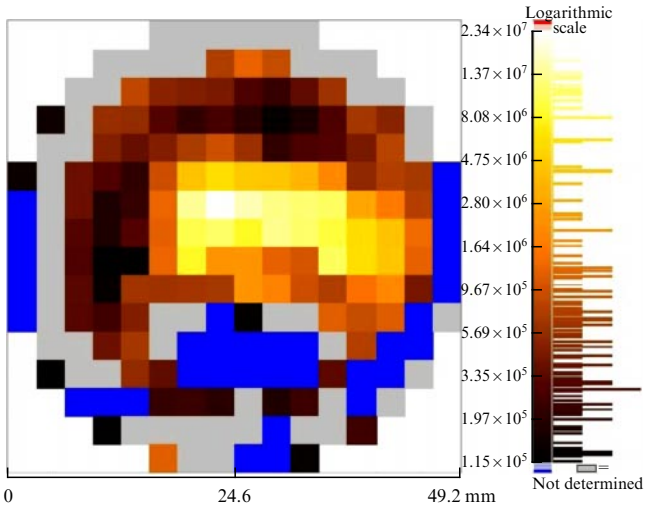

Figure 5. (Color online.) Map of the distribution of specific resistance of a silicon-carbide plate; the mean is 5.4×10^5 Ω cm.

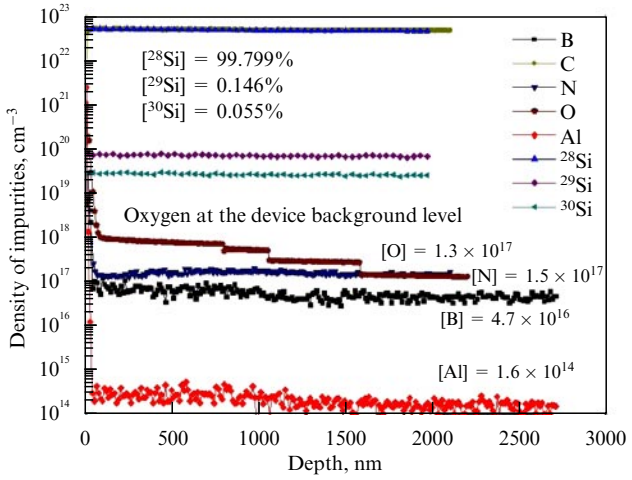

Figure 6. (Color online.) Densities of impurities in an SiC crystal enriched in the ^{28}Si isotope that are determined using the SIMS method.

in the grown crystal should be noted. A concentration this low can be explained by high-quality purification of this isotopic silicon at the gas-centrifuge separation stage.

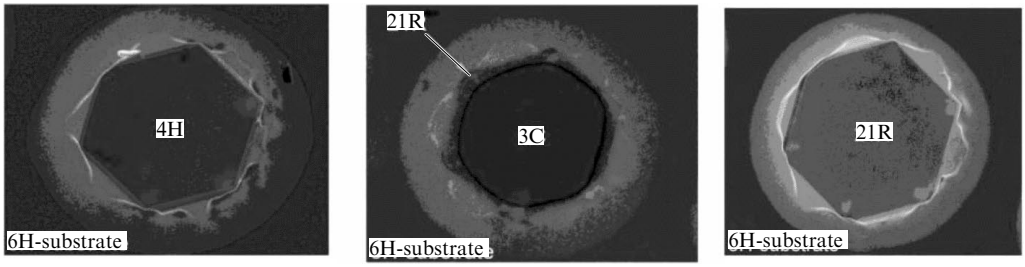

Figure 7. (Color online.) Luminescent SiC crystals of various polytypes grown on 6H-SiC-polytype seeds. The crystals were doped in the process of growth with nitrogen and gallium.

Examination of the isotope-enriched SiC crystals enabled determining the fine structure of the silicon vacancy center [19].

3.1.2 Growing SiC crystals of various polytypes. The technique developed enabled the production of high-purity SiC crystals belonging to various polytypes, including 4H [29], 6H, and 15R [30]. These crystals were used to study the structure of vacancy centers that are of interest for creating efficient sources of individual vacancies.

SiC crystals belonging to a definite polytype were grown in various ways:

(1) on a substrate of the required polytype. For example, polytype-4H crystals were grown on substrates of the same polytype. To increase the polytype reproducibility, so-called off-axis seeds were used whose angle of deviation from the basal plane was 4–8°;

(2) on seeds of any polytype; however, the crystal was grown under conditions that facilitate the creation of a particular polytype. We have found a correlation between the polytype structure and deviation from stoichiometry, whence it follows that cubic polytypes (3C, 8H, and 21R) are produced under a relative excess of silicon, while hexagonal polytypes (4H and 27R) are more likely to be produced under a relative excess of carbon [31].

It was also shown that rhombohedric polytypes are more stable if they are grown in the [0001]Si direction rather than in the [0001]C direction. This and other observations enable controlled growth of some rare polytypes on substrates made of widespread polytypes (Fig. 7).

3.2 Decreasing the content of structural defects in the crystal grown

The density of micropores and dislocations in the crystals grown was measured using the optical method and the results

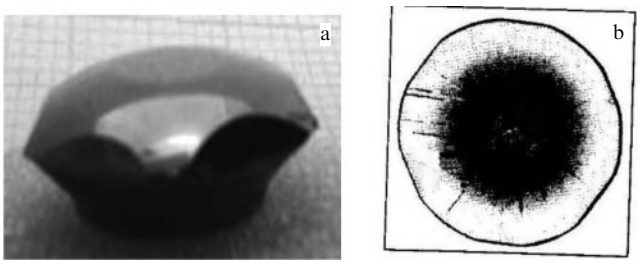

Figure 8. (a) Crystal obtained by the lateral overgrowth method. (b) A plate cut off from that crystal was etched in a KOH melt to decorate edge dislocations directed perpendicular to the crystal surface.

from optical etching in a KOH alkali melt. The measurements showed that the average density of micropores in the SiC crystals grown does not exceed 3 cm^{-2}, while the dislocation density ranges from 10^3 cm^{-2} to 10^4 cm^{-2}.

We have shown that the dislocation density in the SiC crystals grown can be significantly reduced. For example, the dislocation density was greatly diminished if the crystal seed was laterally overgrown [32–34]. The reduction in the dislocation density in the overgrown area of the crystal is illustrated in Fig. 8. The dark color in the crystal center is due to the high density of dislocations. The peripheral part of the plate displays only individual etch pits due to dislocations. The dislocation density in this area does not exceed 10 cm^{-2}, i.e., it is two to three orders of magnitude smaller than in the center of the crystal.

Another method for obtaining low-dislocation SiC crystals was proposed in [35, 36]: it amounts to using special seeds with a profiled surface (Fig. 9).

We note that the density of etch pits in the grown layer above the mesastructure site is not significantly affected. An explanation is that the dislocations that are present in the seed

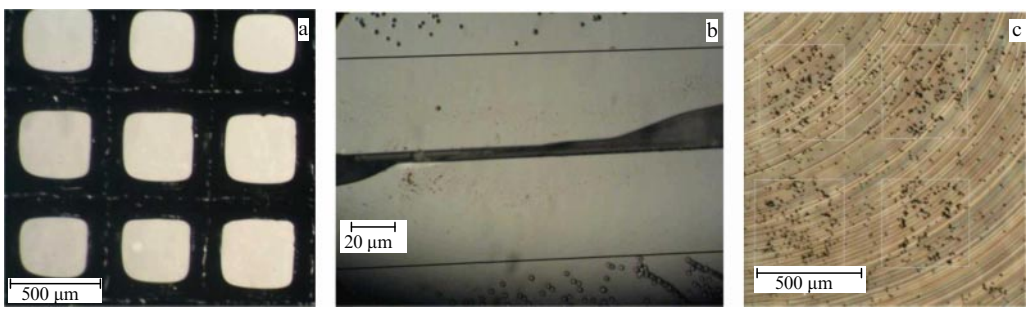

Figure 9. Seed surface with mesastructures observed in reflected light (a) prior to and (b) after the end of growth on a (0001) Si face and (c) subsequent etching in a KOH melt. Growth temperature is $T = 2050\,^{\circ}C$ and the growth time is (b) 1 h and (c) 10 h. Lines indicate boundaries of mesastructure sites. The images were made using a Nomarski microscope in the mode of crossed polarizers.

crystal primarily propagate into the growing layer. The density of the etch pits in the crystal area above the groove (Fig. 9b) is significantly (by two orders of magnitude or more) lower than in the main crystal matrix. The sharp decrease in the dislocation density can be explained in the case of unimpeded lateral overgrowth by the absence of stress-risers (growth steps and aggregation of impurities) that impede displacement of the layer and a relatively high energy of dislocation climb.

We note that micropores are virtually completely absent in overgrown areas. The emergence of micropores in SiC is known to be primarily initiated by screw dislocations with a large Burgers vector, the occurrence of which is unlikely in the case of unimpeded overgrowth. Dislocation micropores can merge and annihilate each other, as a result reducing their average distribution density. An etch pit whose diameter is over 15 μm corresponds to a micropore, while a diameter of less than 15 μm indicates a dislocation.

Using data on changes in the dislocation density in epitaxial growth on mesastructures, we grew a crystal for a long time to examine how the bulk crystal quality can be improved: the duration of growth was increased to 10 h, with a normal growth rate of 100 μm h^{-1}.

The results are shown in Fig. 9c. It is clearly seen that etch-pit aggregates follow the location and boundaries of mesa-structures that existed prior to the beginning of the growth process. The pit density above the mesastructures corresponds to the initial density in the seed crystal, about 5×10^4 cm^{-2}. A significant reduction in the etch-pit density (by two orders of magnitude) is observed between the mesastructure sites. Figure 9c shows that the dislocation density above the grooves that are fully overgrown is not zero. The generation of new dislocations can be due to the mechanical stresses that emerged in the seed crystal in preparing the mesastructure.

The results obtained enable us to draw the following conclusions.

(1) The dislocation density in SiC layers grown on the protruding areas in the absence of normal-growth steps is lower than that on a usual unprofiled surface. This phenomenon is apparently related to the absence of growth steps on the surface: stress occurs that facilitate dislocation growth.

(2) The probability of inheriting edge dislocations perpendicular to the surface, which are already available on the substrate, remains high within the boundaries of the protruding area.

(3) A sharp decrease in the density of edge dislocations perpendicular to the surface is observed in the case of unimpeded lateral overgrowth.

We have described realistic approaches to significantly improving the quality of crystals. The dislocation density decreases in the case of lateral overgrowth of crystals or protruding surface fragments under the condition that the edge dislocations perpendicular to the surface, which are available in the crystal, are barely inherited. The reduced dislocation density persists if crystal growth is extended in time.

4. Development and studies of high-voltage power and pulse 4H-SiC-based diodes

The range of applications of devices based on materials with a large bandgap width and, primarily, those based on 4H-SiC can be expected to expand in the nearest future [37]. High-voltage 4H-SiC diodes and switching-type 4H-SiC transistors are promising for developing a broad nomenclature of small-size power converters that endure high power density owing to the high conversion rate, the high permissible operation temperature, and a simplified cooling system. High-voltage pulse 4H-SiC diodes will enjoy high demand in new communications and data transfer systems (pulse superbroadband radio), superbroadband radar locators, and pulse power-engineering systems.

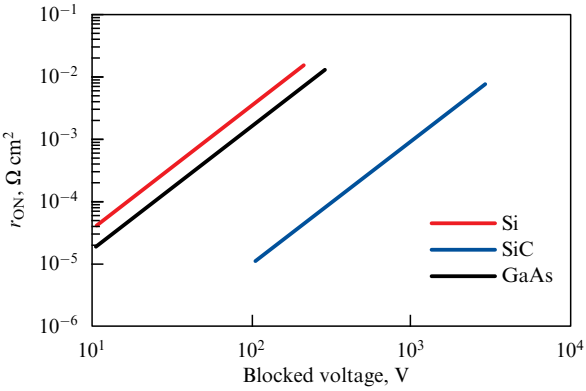

Figure 10. (Color online.) Comparison of the blocking capacity and forward resistance of SDs based on Si, GaAs, and 4H-SiC; r_{ON} is the specific resistance in the open state.

4.1 Power Schottky diodes with an integrated Schottky p–n structure

Schottky diodes (SDs) based on 4H-SiC are gradually replacing silicon-based high-voltage fast-recovery diodes (FRDs). The main disadvantage of silicon FRDs is that they operate with injection of minor carriers, while the buildup of minor carriers in a device limits its switching rate. Although existing silicon SDs operate without injection and switch rapidly, the reverse voltage that they can block does not exceed 200 V. The avalanche breakdown field in 4H-SiC is an order of magnitude larger than in silicon. Owing to this, a higher reverse voltage is attainable together with a rather high level of doping of the blocking base, and the higher doping level in turn ensures a relatively small resistance in the conducting direction. A comparison of the blocking capacity and conducting-direction resistance of 4H-SiC SDs with those of silicon and arsenide-gallium diodes is shown in Fig. 10.

If resistance is limited from above by 10 mΩ cm^2, the maximum reverse voltage for silicon and arsenide-gallium diodes is about 200 V, while 4H-SiC SDs can block a voltage of several kilovolts. These diodes can operate at higher temperatures and endure a larger thermal load owing to the large bandgap width and thermal conductivity of 4H-SiC.

To implement the advantages of 4H-SiC in Schottky diodes in practice, we have (1) developed a model to calculate the Schottky barrier height on an actual SiC surface [38]; (2) developed methods to engineer stable Schottky contacts with a tunable-height barrier [39–41]; (3) created a planar protection system to remove premature edge breakdown [42–44]; (4) determined physical mechanisms of leakage under reverse voltage [45–47]; and (5) developed an integrated Schottky p–n structure (JBS) to partly suppress leakage currents [48, 49].

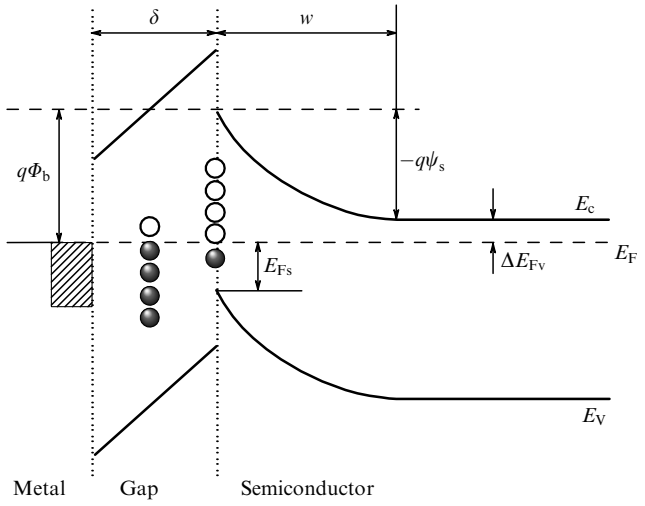

Figure 11. Equilibrium energy diagram of the metal–oxide–semiconductor contact with a uniform spatial distribution of traps in the intermediate dielectric layer.

4.1.1 Schottky barrier height on an actual SiC surface (simulation). Schottky barrier height on a metal–semiconductor interface is known to be usually weakly dependent on the nature of the metal: the bending of energy bands near the semiconductor surface is determined to a greater extent not by the difference between the work functions of the metal and semiconductor but by the charge captured by electron states on the metal–semiconductor interface [50]. An important role is played there by a thin dielectric layer that separates the metal from the semiconductor (e.g., natural oxide on the semiconductor surface). The finite gap width is of importance because if this width tended to zero, the metal would completely shield the surface charge, and the barrier height would be determined by the difference between the work functions of the metal and semiconductor, becoming independent of the presence of surface states. It is generally believed that traps are localized in the plane that separates the dielectric and the semiconductor. But if it is assumed that the layer consists of a natural oxide, 'strict' localization of the traps in the interface plane seems to be unrealistic. For example, a rather extended SiO_x layer (up to several dozen Angstroms below the silicon surface) is observed in thermally oxidized silicon, in which the 'oxidation defects' (so-called P_b centers) make a decisive contribution to the density of states on the SiO_2/Si interface [51].

We have calculated in [52] how the barrier height Φ_b depends on the work function Φ_m of the metal for Schottky contacts based on silicon carbide. It was assumed that the actual surface of SiC is covered with a natural oxide layer whose width can vary from 6 to 20 Å, and traps are distributed uniformly in that layer. We also made the assumption that coating with metal does not result in the emergence of additional traps on the interface. This implies that the only effect of the metal is to redistribute the potential in the structure due to the charge induced on its surface. Finally, it was assumed that the intermediate layer is transparent (in a tunnel manner) to electrons, and therefore the traps can easily exchange electrons with the metal. An energy diagram of the contact between a metal and an n-type semiconductor that takes these assumptions into consideration is shown in Fig. 11 (for the case $\Phi_m - \chi = 0$, where χ is the electron affinity of the semiconductor).

In the diagram shown in Fig. 11, the Schottky barrier height is

$$\Phi_b = |\psi_s| + \frac{\Delta E_{Fv}}{q}\,, \tag{4.1}$$

where ψ_s is the bending of the energy band in the semiconductor and ΔE_{Fv} is the position of the Fermi level in the semiconductor area electrically neutral with respect to the conduction band bottom. To determine ψ_s, we integrated the Poisson equation, which, for the near-surface space charge area (SCA) in the semiconductor and the intermediate layer, decomposes into two equations

$$\frac{d^2\psi}{dx^2} = -\frac{qN}{\varepsilon_s}\,, \qquad 0 < x < w\,, \tag{4.2}$$

$$\frac{d^2\psi(x)}{dx^2} = -\frac{q}{\varepsilon_0\delta}\int_0^{E_{Fs}-q\psi(x)} D_t(E)\,dE\,, \qquad -\delta < x < 0\,, \tag{4.3}$$

where $\psi(x)$ is the potential measured relative to the neutral-area potential, q is the electron charge, w is the SCA thickness in the semiconductor, ε_s is the dielectric permeability of the semiconductor, ε_0 is the dielectric permeability of the intermediate layer, $D_t(E)$ is the energy distribution of the surface-state density in the semiconductor bandgap, and E_{Fs} is the position of the Fermi level on the surface of the semiconductor relative to the upper edge of the valence band. The boundary conditions for Eqns (4.2) and (4.3) are $\psi(w) = 0$ and $\psi(-\delta) = -(\Phi_m - \chi)$.

The problem was solved using a combination of numerical methods. The Runge–Kutta method for solving second-order differential equations $y'' = F(x, y, y')$ was used. According to this method, initial values of the function y_0 and its derivative y_0' should be specified at the point $x = x_0$. In the case under consideration, $x_0 = 0$, $y_0(0) \equiv \psi_s$, and $y_0'(0) \equiv -E(-0)$, where $E(-0)$ is the electric field that has a discontinuity on the dielectric–semiconductor interface. The field $E(-0)$ can be easily expressed in terms of the potential ψ_s as

$$-\psi_s = \frac{qNw^2}{2\varepsilon_s}\,, \quad E(+0) = \frac{2\psi_s}{w}\,, \quad E(-0) = \frac{\varepsilon_0}{\varepsilon_s}\,E(+0)\,. \tag{4.4}$$

Integration of the Poisson equation for the intermediate layer thus involves the value of ψ_s that was chosen such that the solution at the integration range end takes the value $\psi(-\delta) = -(\Phi_m - \chi)$ as a result of integrating Eqn (4.3) from $x = 0$ to $x = -\delta$. For this, first, the corresponding search interval was selected, and the ψ_s value was found in the search interval using the 'interval halving' method.

In calculating the functions $\Phi_b(\Phi_m)$, the shape of the energy distribution of acceptor states was assumed to be Gaussian, with the maximum located in the upper half of the SiC bandgap 1.2 eV lower than the conduction band bottom [53]:

$$D_t(E) = D_{tm}\exp\left[-\frac{(E - E_m)^2}{2(\Delta E)^2}\right]. \tag{4.5}$$

The distribution parameters $D_{tm} = 3 \times 10^{13}$ eV^{-1} cm^{-2} and $\Delta E = 0.14$ eV were chosen such that the integral density of those traps is approximately 2×10^{12} cm^{-2}, and the states themselves are close to single-energy ones. Figure 12 shows the functions $\Phi_b(\Phi_m)$ calculated using the model described

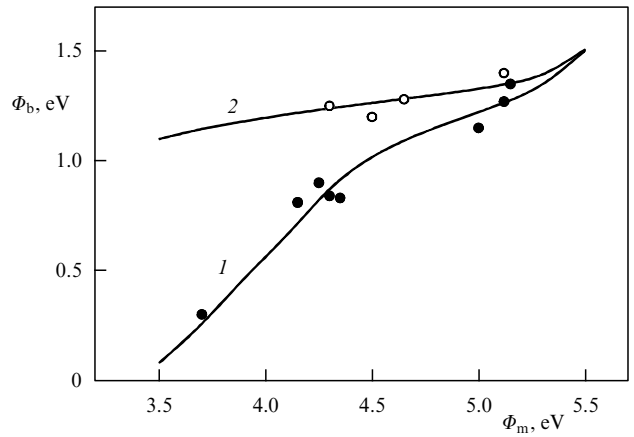

Figure 12. Height Φ_b of the barrier formed on an actual SiC surface as a function of Φ_m, the work function of the metal. The dielectric gap thickness is $\delta = 6$ Å (curve *1*) and $\delta = 20$ Å (curve *2*).

above. The gap thickness was set to be $\delta = 6$ Å (curve *1*) and $\delta = 20$ Å (curve *2*). The same figure displays some selection of experimental data from studies where special measures were taken to remove the natural oxide [54] and from experiments where SiC specimens were subject to high-temperature annealing prior to coating with metal [55].

In accordance with expectations, the dependence $\Phi_b(\Phi_m)$ calculated for $\delta = 6$ Å is steeper than that for $\delta = 20$ Å. This phenomenon can be explained in qualitative terms by the shielding effect of the metal. We can see that the experimental data (shown by dots in Fig. 12) are well described by the calculated dependences. The thicknesses of the natural oxide layer that were chosen for the calculations are quite realistic regarding the conditions under which the structures were prepared.

4.1.2 Forming stable Schottky contacts. One of the problems in Schottky contact technology is the reproducibility and stability of their properties. To stabilize properties of Schottky contacts, various methods have been proposed, including preprocessing the surface prior to coating with metal, rapid thermal annealing (RTA), and deposition of barrier contacts in a vacuum or an inert environment.

We produced Schottky contacts (W, Cr, Ni, Mo, Ti) by electron-beam deposition of a metal in a high vacuum (the metal layer thickness was about 100 nm). Natural oxide was etched immediately prior to coating using an ion (Ar^+) gun. The barrier height ranged for various metals from 1 eV to 1.3 eV, and the perfection factor varied within the range 1.04–1.06. The effect of RTA annealing in a vacuum (for 2 min at a temperature of 600–800 °C) on the dispersion of electric parameters of 4H-SiC Schottky barriers was studied in [41]. (Due to the nonuniformity of Schottky contacts, a dispersion of the voltage drop is usually observed for some fixed direct-current values.) The change in the voltage drop as a result of annealing can be used as a criterion of improvement/degradation of the interface uniformity, while changes in the average statistical voltage drop can serve as a measure of changes in the barrier height.

Figure 13 shows the measured voltage drop (at the current of 100 nA) for W, Mo, Cr, and Ni contacts (50 pieces in each group) not subject to thermal processing (Fig. 13a) and annealed at a temperature of 700 °C (Fig. 13b). The tungsten, chrome, and molybdenum contacts exhibited qualitatively similar behavior: the average barrier height diminished after annealing, and the uniformity of the contact structure was significantly improved (especially in molybdenum contacts). But nickel contacts exhibited a quite opposite trend: the average barrier height increased, and the uniformity of the contact structure significantly deteriorated.

We assume that the decrease in the barrier height and improvement in the contact uniformity observed in the case of tungsten, chrome, and molybdenum are due to homogenization of the interface and modification of surface states (no significant chemical reaction between metal and silicon carbide as a result of RTA annealing at 700 °C has occurred yet [56]). In the case of nickel, a chemical reaction involving production of nickel silicide (Ni_2Si) occurs at a temperature of 700 °C rather actively [57], as a result of which the average barrier height increases. However, for continuous silicide to be formed (and hence for the uniformity of the contact structure to increase), higher temperatures and/or longer duration of annealing is needed.

4.1.3 Planar protective system. To diminish the edge electric field density in planar high-voltage 4H-SiC devices, 'floating' protective rings are frequently used that are formed by local ion implantation of acceptors. In our work, we used ion implantation of boron to form protective rings. If 4H-SiC layers in which boron is implanted at room temperature are thermally annealed, the implanted atoms are noticeably speeded up due to nonequilibrium diffusion stimulated by

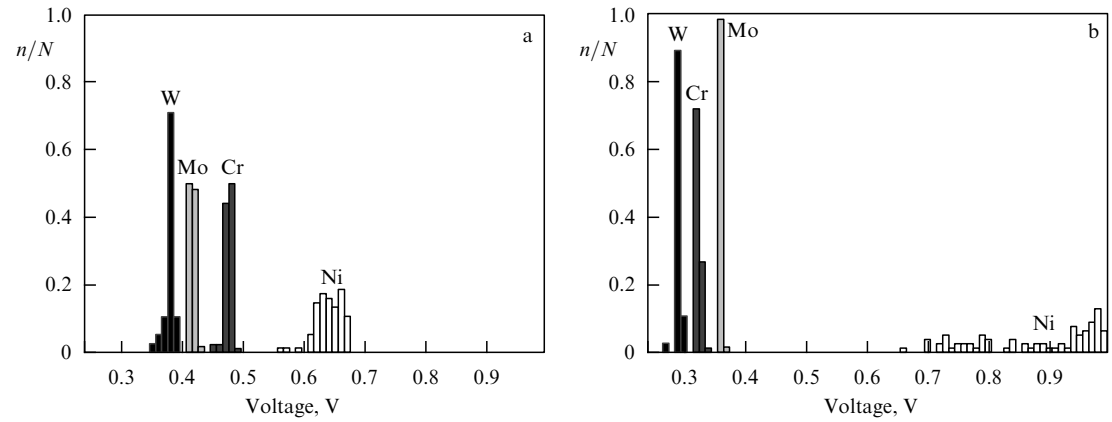

Figure 13. Normalized histograms of the distribution of 4H-SiC Schottky barriers (a) unprocessed and (b) thermally processed at 700 °C by the voltage drop measured at a forward current of 100 nA.

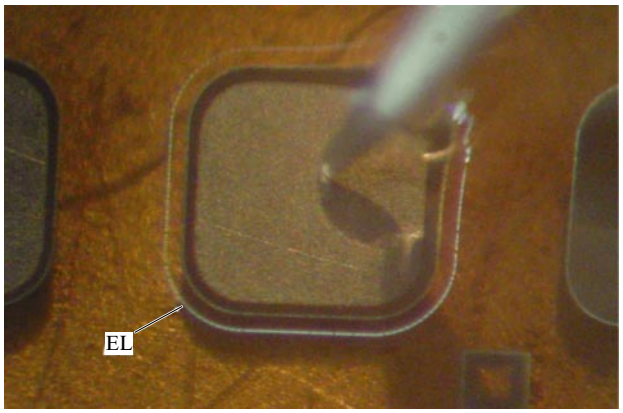

Figure 14. Electroluminescence (EL) on the edge of the protection p–n junction in the breakdown mode.

radiative damages. As a result, the depth of boron-implanted p–n junctions in 4H-SiC significantly exceeds the depth to which ions penetrate in the process of implanting. This has a positive effect on forming the diffusion protective rings: implanting boron rather than aluminum makes the required increase in the breakdown voltage a less challenging problem.

In [42, 43], we studied the breakdown of planar 4H-SiC p–n junctions formed using local implantation of boron ions with an energy of 350 keV. It was shown that owing to nonequilibrium diffusion of boron during post-implantation annealing, the depth of the p–n junction is 1.7 μm, a value that is approximately 1 μm larger than the mean free path of boron ions with an energy of 350 keV in 4H-SiC. The maximum reverse voltage of the p–n junction was restricted by edge avalanche breakdown in the cylindrical part of the p–n junction where the electric field is concentrated. Intense electric luminescence was observed at that area in the breakdown mode (Fig. 14). The breakdown voltage, about 900 V, proved to be close to the calculated breakdown voltage of a planar junction with a 'pierced' base [58]. The calculated value is 990 V for a density 2×10^{15} cm^{-3} of impurities in the n-layer, the n-layer thickness of 12 μm, and the junction curvature radius of 1.7 μm. However, the calculated breakdown voltage of a planar p–n junction ($V_{\rm Bpp}$) with the same parameters of the epitaxial layer is about 2500 V. This implies that the breakdown voltage can be at least doubled in principle. To increase the breakdown voltage further, we used a system of 'floating' protective rings.

Gaps between the main junction and the first ring and the gaps between rings are chosen in a system with 'floating' protective rings such that the space charge areas of the main and floating junctions begin touching each other as anode voltage increases. As a result, the SCA thickness gradually decreases beyond the anode edge, thus facilitating the leveling of the electric field distribution in this area (Fig. 15).

Choosing the number of rings and gaps between them enables implementing the simplest version of such a setup where breakdown occurs not on the edge of the main junction but on the edge of the last ring. The anode potential (relative to the grounded cathode substrate) in this configuration is, in the case of breakdown, such that $V_{\rm BA} > V_{{\rm R}n} = V_{\rm Bcyl}$, where n is the number of rings, $V_{{\rm R}n}$ is the potential of the last ring, and $V_{\rm Bcyl}$ is the breakdown potential of the planar junction in the absence of protection.

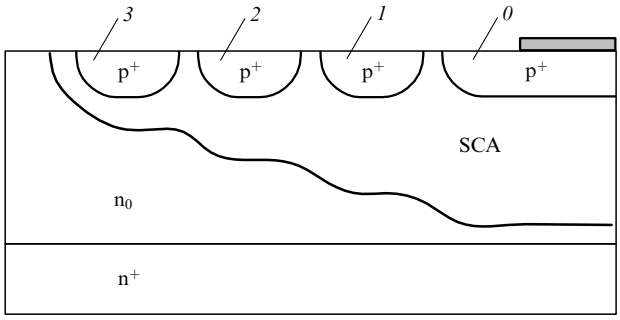

Figure 15. The concept of 'floating' protection rings: *0* is the primary planar p–n junction; *1–3* are the 'floating' rings.

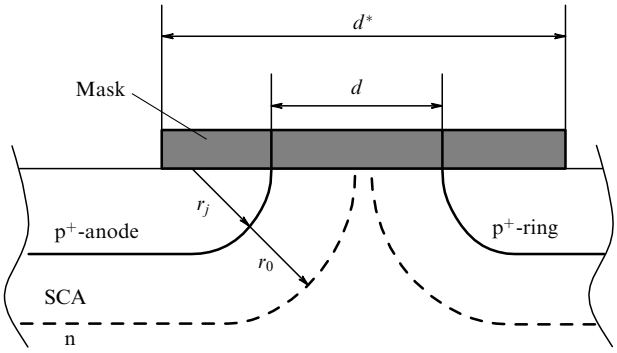

Figure 16. Geometry of protection rings.

The gap d between the rings is chosen such that if the anode voltage is zero, the SCAs of the main and floating junctions are 'almost' touching each other. The d value was chosen in our case somewhat larger than $2(r_0 - r_j)$, where r_0 is the SCA curvature radius at zero bias and r_j is the curvature radius of the metal boundary of the p–n junction (Fig. 16).

The value of r_0 can be found for a cylindrical junction as a solution of the transcendental equation [59]

$$V_{\rm bi} = \frac{qN}{2\varepsilon}\left(\frac{r_j^2 - r_0^2}{2} + r_0^2 \ln\frac{r_0}{r_j}\right), \tag{4.6}$$

where $V_{\rm bi}$ is the contact potential difference in the p–n junction, q is the elementary charge, N is the donor density in the base, and ε is the dielectric permittivity of the semiconductor. Setting $r_j \sim 1.7$ μm and $N = 2 \times 10^{15}$ cm^{-3}, we obtain $r_0 = 2.8$ μm, whence $d \geqslant 2.2$ μm.

The number of rings should be chosen such that in the case where $V_{{\rm R}n} = V_{\rm Bcyl}$, the anode potential does not exceed the breakdown voltage $V_{\rm Bpp}$ of the planar junction. Similar analytic expressions for the ring potential $V_{\rm R}$ as a function of the anode potential $V_{\rm A}$ are reported in [60], where a planar p–n junction with one 'floating' protective ring was studied. This dependence for the 'pierced'-base structure has the form

$$V_{\rm R} = V_{\rm A}\left(\frac{W}{W + kd}\right) - \sqrt{V_{\rm PT} V_{\rm RT}}, \tag{4.7}$$

$$V_{\rm PT} = \frac{qNW^2}{2\varepsilon}, \quad V_{\rm RT} = \frac{qN(kd)^2}{2\varepsilon}, \tag{4.8}$$

$$k = \left[\left(1 + \frac{r_j}{d}\right)^2 \ln\left(1 + \frac{d}{r_j}\right) - \left(\frac{1}{2} + \frac{r_j}{d}\right)\right]^{1/2}. \tag{4.9}$$

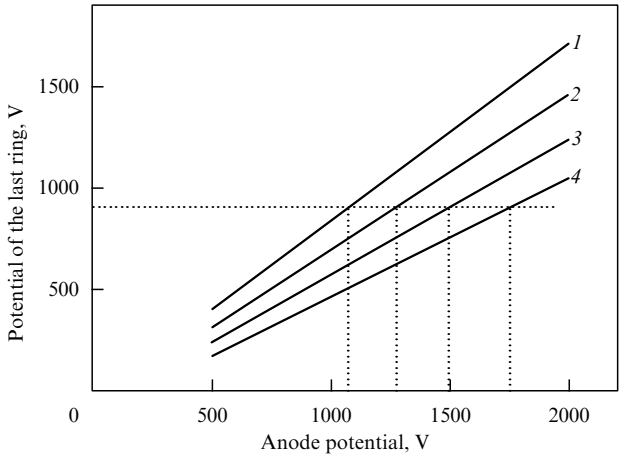

Figure 17. Potential (*1–4*) of the last ring as a function of the anode potential calculated for one to four rings.

Here, W is the base thickness, V_{PT} is the base breakdown voltage, and V_{RT} is the voltage of 'touching'. If the number of rings is greater than one, the potential of the last ring (for a given anode potential) can be calculated as follows. First, the equations given above are used to calculate the potential of the first ring. The first ring is then regarded as the 'main junction', and the same formulas are used to calculate the potential of the second ring. The procedure is iterated until the last ring. It is repeated afterwards for the next value of the anode potential. This approach can be used to find the function $V_{Rn}(V_A)$ for various n.

Figure 17 shows the functions $V_{Rn}(V_A)$ that we calculated for $N = 2 \times 10^{15}$ cm^{-3}, $W = 12$ μm, and $r_j = 1.7$ μm; the number of rings n varied from *1* to *4* and the gap was $d = 2.5$ μm. The calculated results predict that if $V_{Bcyl} = 900$ V, one ring is expected to increase the breakdown voltage to 1070 V, two rings to 1270 V, three rings to 1490 V, and four rings to 1750 V.

Experimental 4H-SiC p–n structures were formed using an epitaxial material with the donor density $N = 2 \times 10^{15}$ cm^{-3} in the n-layer and the n-layer thickness $d = 12$ μm. The main junction and the rings were formed concurrently. The number of rings was chosen to be four. The production mask width d^* for implantation that ensures the $d = 2.5$ μm gap was chosen to be 6 μm (see Fig. 16), given that boron is speeded up due to diffusion in the process of annealing the implanted layer not only in the vertical direction but also in lateral directions (to a distance of about 1.7 μm according to our estimates). ^{11}B ions were implanted into the n-layer in two doses with different energies (at room temperature): (1) a dose of 6×10^{13} cm^{-2} at an energy of 350 keV and (2) a dose of 3×10^{13} cm^{-2} at an energy of 200 keV. Post-implantation annealing was performed at a temperature of 1500 °C in an argon atmosphere for 60 minutes. Contacts with the cathode (substrate) and anode were respectively made of nickel and titanium. Breakdown started to develop at a voltage of about 1800 V (test junctions without protection exhibited a breakdown voltage of about 900 V) and thus attained 72% of the breakdown voltage calculated for a planar p–n junction with the same parameters of the epitaxial layer.

The simplified approach to designing the rings, which is described above, is strictly speaking not optimal from the perspective of attaining the maximum breakdown voltage (the breakdown in the picture described above remains the edge breakdown). To further increase the breakdown voltage, the number of rings should apparently be increased and the distance chosen between them should be variable.

4.1.4 Leakage currents. Reverse current in high-voltage 4H-SiC SDs not infrequently turns out to be 'excessive'. Excessive leakage currents can be caused by quite different reasons: defects in the semiconductor, a nonuniform barrier height distribution over the contact area, design features of diodes that result in premature edge breakdown, etc. Statistical measurements of leakage currents in commercial diode chips CPW3-1700S010 designed for a reverse voltage of 1700 V and forward current 10 A were reported in [47]. To ensure statistical significance, measurements were made for a rather large number of chips, 147 pieces in total. The leakage currents were measured for a fixed reverse voltage of 1400 V at room temperature. Figure 18 shows a classification of the chips by leakage currents.

Dispersion turned out to be rather significant: the values ranged from 10 nA to 6 μA (spanning almost three orders of magnitude). This observation alone is indicative of the defect-related nature of leakage currents. An assumption was made earlier in some studies that the reverse current flow involves penetrant dislocations (see, e.g., [61, 62]), whose density in commercial epitaxial materials is still high, up to $\sim 10^4$ cm^{-2}. It is quite probable that the observed reverse current flows in places where dislocations emerge on the semiconductor surface.

We proposed a mechanism of leakage involving dislocations in [45]. According to this model, the reverse current flows as currents limited by space charge (CLSCs) owing to monopolar injection of electrons from pointlike areas located within the Schottky contact (where penetrant dislocations emerge on the surface) to the semiconductor SCA. The energy barrier for the electrons that leave the metal can be lowered in places where dislocations emerge on the surface and can be shifted from the semiconductor surface to some distance inward from the semiconductor. As a result, a pointlike 'reservoir' of electrons emerges in the near-surface area of the semiconductor. If a negative potential is applied to the metal, monopolar injection of electrons occurs from such a nanoscale reservoir to semiconductor SCAs, and the current flows as a CLSC. If the reverse current flows driven by this

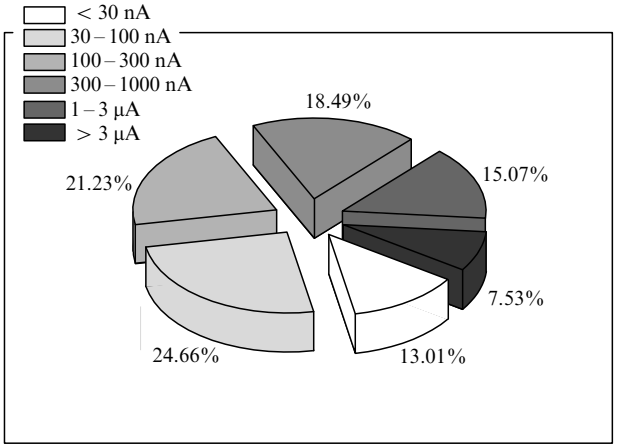

Figure 18. Statistical data on classification of diode chips CPW3-1700S010 by groups as per the leakage current under a reverse voltage of 1400 V (room temperature).

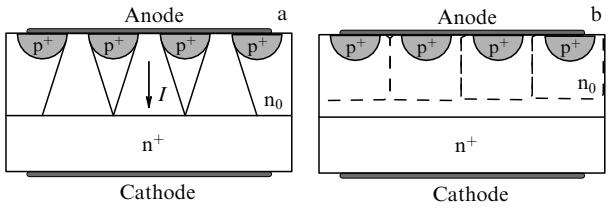

Figure 19. Concept of JBS structure: (a) forward and (b) reverse bias.

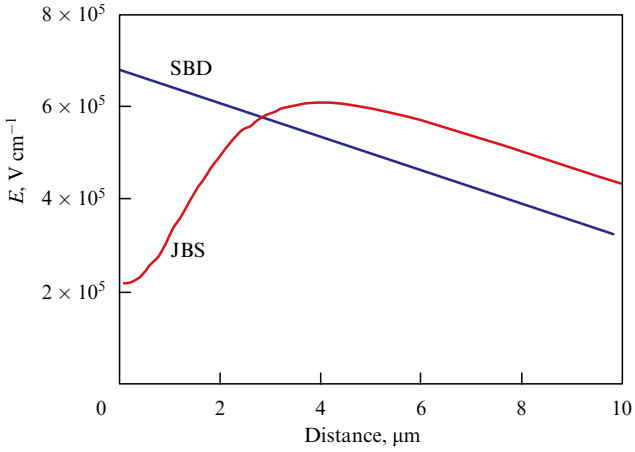

Figure 20. Electric field E in the base of an SBD (Schottky barrier diode) and JBS diode (n-base thickness 10 μm, doping level 2×10^{15} cm^{-3}, voltage 500 V).

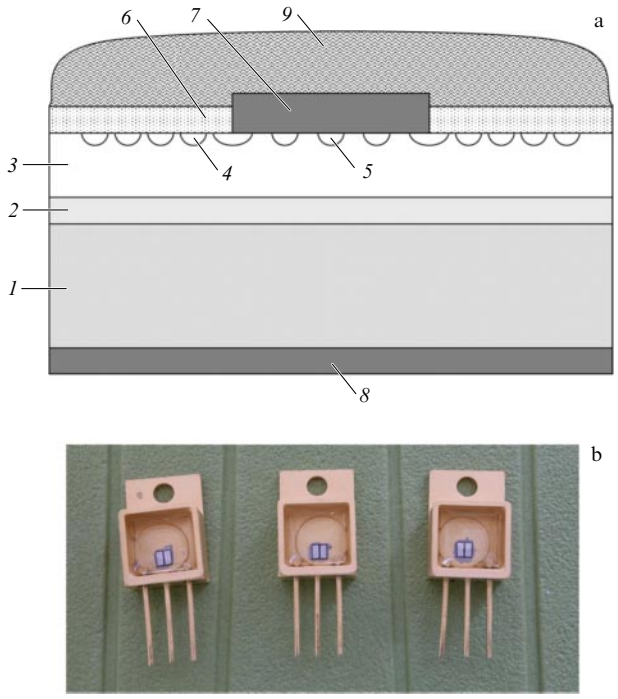

Figure 21. (a) Schematic cross section of a 4H-SiC-JBS diode: *1* is the substrate with n-type conductivity, *2* is the buffer epitaxial n-layer, *3* is the base epitaxial n-layer, *4* are the 'floating' protection p-rings, *5* are the local p-regions of the JBS structure, *6* is the oxide, *7* is the Schottky-contact metal (anode), *8* is the ohmic contact metal (cathode), *9* is a passivating coating. (b) Images of packaged diodes.

mechanism, the current–voltage characteristic (CVC) apparently depends in a complicated manner on the number of dislocations within Schottky areas and on their types. If that is the case, the significant dispersion of leakage currents in the studied chips should become quite clear.

4.1.5 Integrated Schottky p–n structure. Modern 4H-SiC-based SDs are designed as integrated Schottky p–n structures (JBS) in which Schottky areas alternate with local implanted p-areas (Figs 19 and 20). Current flows in the forward direction via the Schottky areas, and therefore the resistance of such a diode in the open state is determined by characteristics of the Schottky contact. At the same time, the gap between the p-areas is made so narrow that if the diode is switched in the reverse direction, SCAs of adjacent p–n junctions touch each other under some voltage. A system of p-areas operates as a result of a shielding mesh: field lines partly terminate on the p-areas rather than on the Schottky metal. Owing to the shielding effect, the maximum-field area in the JBS-structure diode, unlike in normal SD, is not located on the metal–semiconductor interface but is somewhat shifted inward from the surface, thus facilitating the decrease of the reverse current to values characteristic of p–n junctions.

The leakage currents sensitive to the surface field are diminished in the JBS structure. (This also applies to the thermal emission current of electrons from the metal to the semiconductor, the value of which in 4H-SiC-based SDs strongly depends on the surface field [46].) The p-areas in the JBS structure were produced in our studies by means of nonequilibrium boron diffusion from an implanted source concurrently with the formation of protective rings. Figure 21a shows the final design of the diode chip, and Fig. 21b displays a photo of packaged diodes.

In [47], we studied the efficiency of using JBS structures to suppress leakage currents. Some high-voltage test SDs made especially for this purpose contained a JBS structure, while some did not (SBD). Gaps between local p-areas in the JBS-structure SDs varied from 6 to 10 μm.

Most of the produced diodes (including SBDs) could block a reverse voltage of more than 2000 V. To compare leakages in diodes with different topologies, reverse currents were measured under a voltage of 2100 V in 420 diode structures (105 diodes of each type).

Figure 22 displays measured results as histograms of the number of diodes by the leakage-current values. We can see that the leakage current dispersion is large for diodes of each type, indicative of the defect-related nature of leakages. The most probable value of the leakage current I^* is about 3 μA for SBDs, 0.5 μA for JBS3 diodes, 0.3 μA for JBS2 diodes, and 0.1 μA for JBS1 diodes. The I^* value is seen to monotonically decrease in the SBD–JBS3–JBS2–JBS1 sequence, i.e., as the total of Schottky areas in the diodes diminishes. It is of importance that the histograms displayed in Fig. 22 partially overlap due to a significant dispersion of leakage current values (for example, the leakage of 17 JBS2 diodes (of 105) was larger than I^* for JBS3 diodes). Therefore, in discussing a reduction in leakage currents as the gap between p-rings in the JBS structure diminishes, it must be stressed that this conclusion refers to averaged statistical data.

Figure 23 shows the normalized leakage current I^*/I^*_{SBD} as a function of the normalized surface of Schottky areas S/S_{SBD} ($S_{\mathrm{SBD}} = 4.9 \times 10^{-4}$ cm^2). Curve *1* in this figure shows

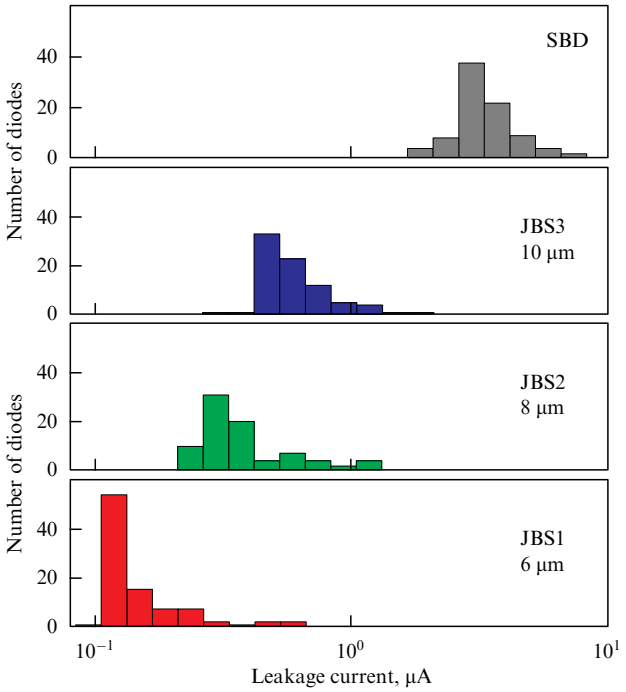

Figure 22. Histograms of the distribution of test diodes by leakage current under a reverse voltage of 2100 V (room temperature).

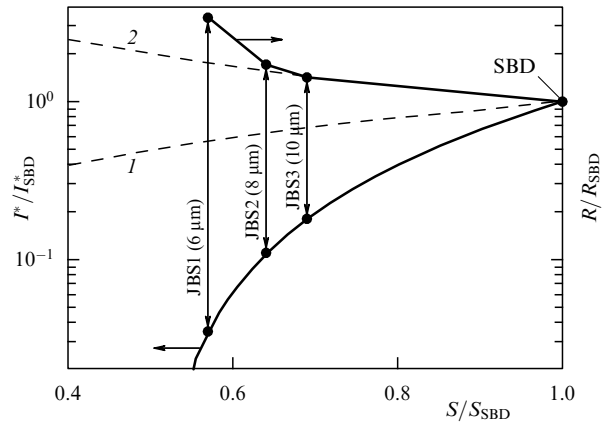

Figure 23. Normalized leakage current I^*/I^*_{SBD} and normalized resistance of test diodes in open state R/R_{SBD} as functions of the normalized surface of Schottky areas S/S_{SBD}.

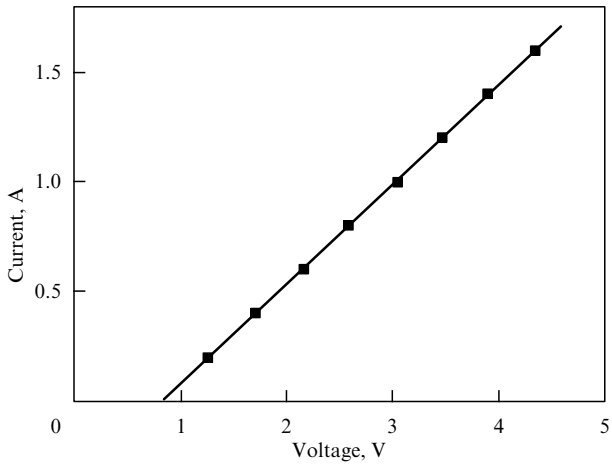

Figure 24. Pulse-forward CVC of a 3300 volt JBS diode in the open state.

the expected dependence when suppression of the leakages is determined solely by a decrease in the total surface of Schottky areas (a purely geometric effect). We can see that if the gap between the p-rings decreases, the leakage current decreases faster than could be expected on the basis of a purely geometric effect. It is quite apparent that a significant role in partial suppression of leakage currents is played not only by the geometric effect but also by electric field shielding in the JBS structure: the smaller the gap between p-rings, the stronger it is exhibited.

However, it should be taken into account that a decrease in the total surface of Schottky areas should result in an increase in the resistance of diodes in the forward direction. Figure 23 shows the normalized resistance of diodes in the open state (R/R_{SBD}) as a function of the normalized Schottky area S/S_{SBD}. Curve *2* in this figure shows the expected dependence in the case where the increase in resistance is only determined by a purely geometric effect. We can see that the increase in resistance in the case of JBS3 and JBS2 diodes is actually driven by the geometric effect. The increase in resistance for JBS1 diodes is much larger than expected, however. An explanation is that the Schottky areas in JBS1 diodes are separated by the space charge regions of implanted p–n junctions. Thus, the JBS structure formed in 4H-SiC SDs using boron implantation facilitates an efficient reduction of leakage currents: if the gap between local p-areas is chosen in an optimal way (8 μm), leakages diminish by almost a factor of 10.

4.1.6 High-voltage (3300 V) 4H-SiC-based JBS diodes. We have made 4H-SiC-based JBS diodes with a maximum reverse voltage of 3300 V [49]. The work area of the diodes (anode contact area) was 1.44 mm^2. The forward CVC was described in a range of currents from 10^{-11} to 1.5 A by the model of thermal emission with the Schottky barrier height $\Phi_b = 1.16$ eV and the perfection factor $n = 1.01$. The differential resistance of the diodes in the open state, $R_s = 2.2\ \Omega$ (Fig. 24), was determined by the resistance of the blocking epitaxial n-base (the impurity density $N = 9\times10^{14}$ cm^{-3}, the n-layer thickness $d = 34$ μm). In the reverse direction, the diodes blocked a voltage of no less than 3300 V (Fig. 25) (the leakage current under a reverse voltage of 3300 V at room temperature was about 1 μm).

Figure 26 shows typical reverse-recovery characteristics measured when diodes were switched from the forward current (*1*: 0.4 A, *2*: 1.2 A) to a reverse voltage of 500 V.

Neither the amplitude of the reverse current nor its decrease with time depends on the forward current in any way. This is direct evidence of a purely capacitive nature of the reverse current. The amplitude of the reverse current is 0.6 A and its flow duration is $\Delta t_r = 20$ ns. The reverse-recovery charge defined as

$$Q_{rr} = \int_0^{\Delta t} I_r\,\mathrm{d}t \qquad (4.10)$$

is about 5 nC. On the other hand, the charge of majority carriers (electrons) taken away from the base after the reverse voltage V_r is applied can be calculated as

$$Q_n = S\sqrt{2q\varepsilon NV_r}\,. \qquad (4.11)$$

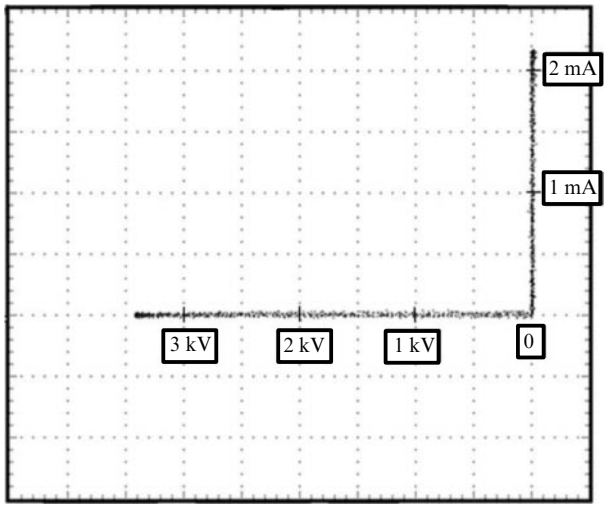

Figure 25. CVC recorded from the screen of a high-voltage characteristic tracer.

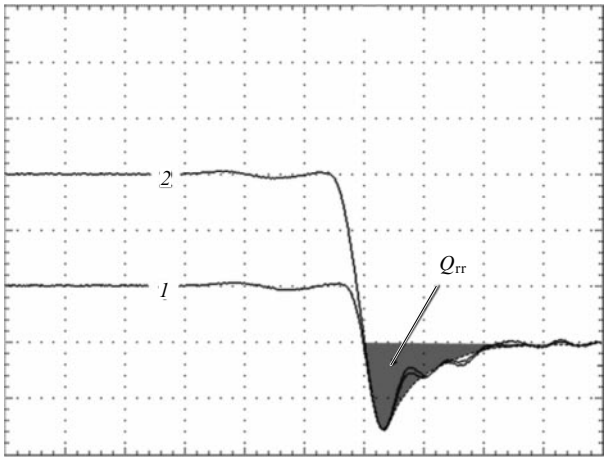

Figure 26. Typical characteristics of reverse recovery recorded from an oscilloscope screen in switching a diode from forward current (*1* — 0.4 A, *2* — 1.2 A) to a reverse voltage of 500 V. The scale for current (the ordinate axis) is 0.4 A per graduation line, and the scale for time (the abscissa axis) is 10 ns per graduation line.

If $V_r = 500$ V, the charge $Q_n = 5.1$ nC calculated using Eqn (4.11) virtually coincides with the charge Q_{rr}.

4.2 Fast-recovery avalanche diodes

Power electronics require diodes that can operate in a controlled-avalanche breakdown mode. Such diodes are required for pulse converters with enhanced requirements for reliability. Avalanche diodes can be used as fast-operating arresters of high-voltage surges that emerge, for example, in circuits containing an inductive load and as super-high frequency (SHF) power suppressors.

The application of avalanche diodes for making high-voltage piles should be noted separately. Avalanche diodes connected in series into a pile enable a more uniform distribution of voltage among reverse-biased diodes and in this way prevent failure of the entire set if overvoltage occurs on a single diode or on more than one diode simultaneously. It is desirable for all applications listed above that the diode operating in the avalanche mode be able to dissipate large power.

Figure 27. 4H-SiC FRAD installed in a low-power casing using soldering with a lead–tin solder. The anode area is 1 mm^2.

In [63, 64], we studied operations of 4H-SiC diodes with a p–n junction in the avalanche breakdown mode. Such parameters as the avalanche diode resistance, the saturated drift velocity of electrons in the blocking n-base in strong fields, and the temperature coefficient of breakdown voltage were determined.

High-voltage fast-recovery avalanche diodes (FRADs) based on 4H-SiC were presented in [65]; they feature a fast response comparable to that of commercial 4H-SiC Schottky diodes and can dissipate an energy of up to 2.9 J cm^{-2} in the individual avalanche pulse mode. The diodes were made based on commercial 4H-SiC n-type plates with epitaxial p- and n-layers. The post-growth technology of manufacturing diodes includes the following steps:

(1) resistance contacts to the upper epitaxial p-layer and n-substrate are formed;

(2) a protection system is formed on the periphery of anode contacts to prevent premature edge breakdown;

(3) a plate with diode structures is cut into chips;

(4) the chips are irradiated with high-energy protons at a unique research facility, the FTI Cyclotron, to reduce the reverse-recovery charge of diodes. (4H-SiC can block high reverse voltage if the base doping level is sufficiently high. Owing to this, 4H-SiC diodes with a p–n junction can also efficiently operate without modulation of blocking-base conductivity by injected carriers. To increase the response speed of diodes, it is reasonable in this case to suppress injection of minority carriers, for example, using proton radiation [66].);

(5) the chips are soldered in a metal-and-glass casing; solder connections of wire leads are arranged, and the casing is filled in with a silicone gel (Fig. 27).

Figure 28a shows a typical forward CVC of diodes (at amperages of up to 10 A) recorded using an L2-100 digital characteristic tracer (data were recorded in the mode of one-off launch of voltage scan). The diode opening voltage in the forward direction is about 2.8 V. (This value is approximately equal to the contact potential difference in the 4H-SiC p–n junction.) The differential resistance of diodes in the open state is about 0.3 Ω. Figure 28b shows a typical reverse CVC of the diodes (with currents of up to 2 mA) recorded using an L2 characteristic tracer. It can be seen that a rapid breakdown of diodes in the reverse direction occurs at a voltage of 1560 V.

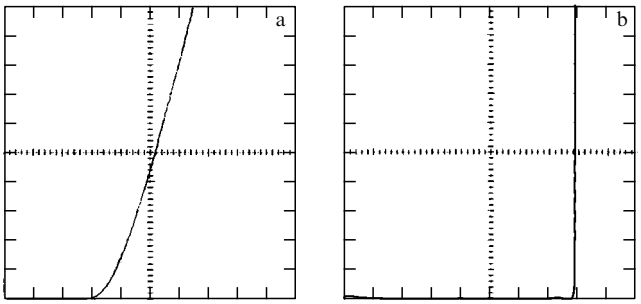

Figure 28. (a) Forward and (b) reverse CVCs of the produced 4H-SiC FRADs. Scale: Fig. a, voltage: 1 V per graduation line, current: 1 A per graduation line; Fig. b, voltage: 200 V per graduation line, current: 0.2 mA per graduation line. p–n junction area is 1 mm^2. Room temperature.

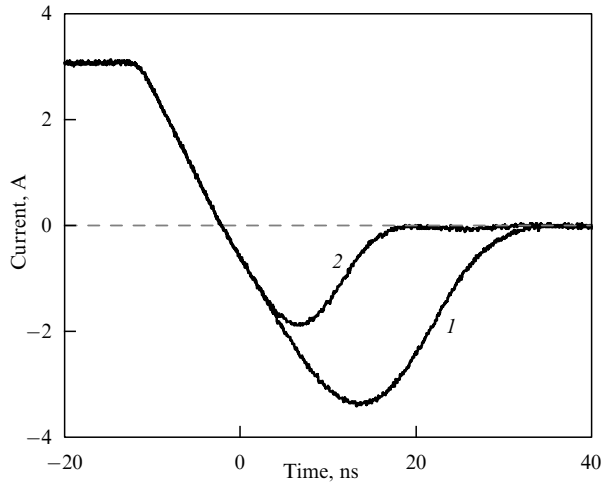

Figure 29. Typical RR characteristics of nonirradiated (curve *1*) and irradiated (curve *2*) diodes in switching from a forward current of 3 A to a reverse voltage of 500 V.

Figure 29 shows typical characteristics of the reverse recovery (RR) of nonirradiated (curve *1*) and irradiated (curve *2*) diodes when they are switched from a 3 A forward current to a reverse voltage of 500 V. (The rate with which the current is switched from the forward direction to the reverse direction is 300 A μs^{-1}.) The respective RR charges of nonirradiated and irradiated diodes were 63 and 20 nC. The diodes preserved a 'soft' character of recovery after irradiation; this is an indication that irradiation primarily results in reducing the injection coefficient of the p–n junction [67]. The respective RR times of the nonirradiated and irradiated diodes were 35 and 20 ns. Proton irradiation is thus an effective tool for improving dynamic characteristics of high-voltage 4H-SiC p–n junctions.

Figure 30 shows failure tests of crafted 4H-SiC FRADs when operated in the pulse avalanche mode. The tests were conducted using an electric setup that was named unclamped inductive switching (UIS) [68]. To increase the power density, small-area diodes were made (4.9×10^{-2} mm^2 with an anode of 250 μm in diameter).

The data displayed in Fig. 30a correspond to a peak avalanche current of 3.5 A (current density 71 A mm^{-2}) and the maximum reverse voltage 1700 V. The oscillograms shown in Fig. 30a are indicative of the reversible character of avalanche breakdown (the diode CVC displayed in Fig. 30b did not degrade after the avalanche pulse had passed). The

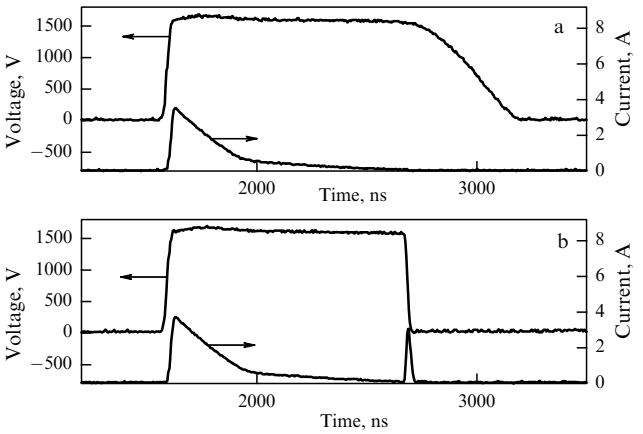

Figure 30. Current and voltage oscillograms measured in the UIS circuit.

peak avalanche current (3.7 A) presented in Fig. 30b is somewhat larger than that in Fig. 30a. A current surge is observed at an instant close to the avalanche-pulse end when voltage drops to zero, which indicates a catastrophic failure of the diode (monitoring of the CVC after the avalanche pulse had passed confirmed that the diode blocking capacity is lost). The avalanche energy calculated using the dependences $I(t)$ and $V(t)$ shown in Fig. 30a is $E_{\mathrm{av,\,max}} = 1.4$ mJ (2.9 J cm^{-2}).

In our opinion, the catastrophic failure of the diode occurred due to electric thermal breakdown. (Electric thermal breakdown of diodes in the reverse direction usually begins with reversible avalanche breakdown, the development of which, as the voltage and current increase, eventually results in irreversible thermal breakdown and destruction of the diode due to imbalance between the power released in the diode and dissipated from it.) Computer simulation of the nonstationary thermal process in the diode in the pulse testing mode described above has shown that the local temperature in the center of the diode base region can exceed 1100 K.

Generally speaking, the operability of semiconductor diodes with the p–n junction under heating has a basic limitation related to an increase in the density of intrinsic carriers as the temperature increases. The critical temperature is the temperature at which the density of intrinsic carriers in the semiconductor becomes comparable to that of dopants in the diode base regions. The intrinsic carrier density in 4H-SiC with a 3.24-eV bandgap is extremely small at room temperature; various estimates show that it is in the range $10^{-8}-10^{-7}$ cm^{-3}. The doping level of the blocking base in high-voltage 4H-SiC diodes is within the range $10^{15}-10^{16}$ cm^{-3}. The intrinsic-carrier density attains values this high if the diode is heated to a temperature of about 1350 K.

In our opinion, this basic limitation on the maximum dissipated energy of an avalanche pulse is realized in the 4H-SiC FRADs we crafted. It is of importance that the response speed of the 4H-SiC FRADs that we produced is not inferior to that of commercial 4H-SiC Schottky diodes (Table 2). In accordance with expectations, pre-breakdown leakages in diodes with a p–n junction are significantly smaller. Although such 4H-SiC FRADs are inferior to Schottky diodes with regard to the forward voltage drop, they may find their niche in the areas listed above.

4.3 Subnanosecond diode circuit breakers

Semiconductor devices that can switch high electric power in the micro-, nano-, and picosecond time ranges are required

Table 2. Comparison of electric parameters of commercial 4H-SiC Schottky diodes CPW4-1200-S005B and 4H-SiC FRADs produced at room temperature.

Parameter	Notation	CPW4-1200-S005B	4H-SiC FRAD
Anode area	S	1.54 mm^2	1 mm^2
Maximum constant reverse voltage	V_{Rmax}	1200 V	1200 V
Forward voltage drop	V_{F}	1.8 V ($I_{\mathrm{F}} = 3$ A mm^{-2})	4.5 V ($I_{\mathrm{F}} = 3$ A mm^{-2})
Reverse current	I_{R}	100 μA mm^{-2} ($V_{\mathrm{R}} = 1200$ V)	0.01 μA mm^{-2} ($V_{\mathrm{R}} = 1200$ V)
RR charge	Q_{rr}	18 nC mm^{-2} ($I_{\mathrm{F}} = 3$ A mm^{-2}, $V_{\mathrm{R}} = 800$ V, $\mathrm{d}I/\mathrm{d}t =$ 200 A μs^{-1})	20 nC mm^{-2} ($I_{\mathrm{F}} = 3$ A mm^{-2}, $V_{\mathrm{R}} = 500$ V, $\mathrm{d}I/\mathrm{d}t =$ 300 A μs^{-1})
Zero-shift capacity	C_0	167 pF mm^{-2}	180 pF mm^{-2}
Avalanche energy	$E_{\mathrm{av,max}}$	—	2.9 J cm^{-2}

for systems of pulse power supply to power lasers, X-ray tubes and accelerators of charged particles, radio navigation and locator systems, fast-process recorders, devices for pulse electric-discharge purification of gaseous exhausts of vehicles and chemical production facilities, systems that supply power to and control the operation modes of converters intended for power supply to gas and oil pumps, etc. Of great interest for the power pulse energy-engineering industry is the pulse system where energy is accumulated in an inductive way and subsequently transferred to a load using superfast breaking of large currents (an important feature of this approach is that the pulse voltage on the load, which emerges when the current is interrupted, can be much higher than the voltage at preceding stages of pulse formation).

Dedicated work conducted at the Ioffe Institute in the early 1980s aimed at studying the physics of the buildup and dispersal of electron–hole plasma in silicon diodes resulted in the development of devices that can interrupt large currents in the nanosecond range. These devices were referred to as sharp-recovery drift diodes (SRDDs) [69].

The operation of high-voltage silicon SRDDs is based on rapid interruption of the reverse current that flows through it after the electron–hole plasma (EHP), which was preliminary pumped into the diode base region by a short pulse of current, has been pumped out. The voltage on the diode very rapidly increases (in a prototype of pulse shaper, the SRDD short-circuits the transfer line from the generator of the pulse to be shaped to the load for the time needed for attaining the required wave amplitude and then rapidly opens the line; the pulse edge in the load is determined in this case by the transient process in the SRDD and its duration is set by the master generator).

Switching SRDDs consists of two characteristic stages. At the first stage, plasma is dispersed relatively slowly, but only a small fraction of the operational voltage drop occurs on the diode at this stage. At the second stage, at the instant when the density of nonequilibrium carriers near the $\mathrm{p-n}$ junction becomes less than the density of the carriers in the blocking base, the reverse-current interruption stage begins, accompanied by SCA expansion into the base. The interruption of current occurs at the maximum rate if the following conditions are satisfied at the beginning of the SCA expansion: (1) nonequilibrium carriers are fully removed from base regions (for this, the design of the diode and parameters of pumping-in and evacuation of the nonequilibrium carriers are chosen depending on the mobility and lifetime of injected carriers); (2) the reverse current is large enough to rapidly recharge $\mathrm{p-n}$ junction capacities. In other words, for SRDDs to operate at the maximum rate, conditions must be created under which the barrier capacity of the blocking $\mathrm{p-n}$ junction is recharged with a large initial bias current.

Currently available generators based on individual silicon SRDDs generate pulses with an amplitude of up to 1300 V under a 50 Ω load, with the respective leading and trailing edges equal to 2 and 5 ns (repetition rate up to 100 kHz).

According to estimates, the use of 4H-SiC can significantly improve the main SRDD parameters, namely, the operation speed, the specific switched power, and the clock rate of pulses. The rate of voltage rise in SRDDs is limited from above by the value $(\mathrm{d}U/\mathrm{d}t)_{\max} = E_{\mathrm{b}} v_{\mathrm{sat}}$, where E_{b} is the strength of the avalanche breakdown field in the semiconductor and v_{sat} is the saturated velocity of carrier drift. For Si diodes, $(\mathrm{d}U/\mathrm{d}t)_{\max} = 2 \times 10^{12}$ V s^{-1}, while for SiC diodes, $(\mathrm{d}U/\mathrm{d}t)_{\max} = 6 \times 10^{13}$ V s^{-1}, a value that is almost thirty times larger. This implies in practice that, for example, the duration of the voltage growth front in the case of a 4H-SiC SRDD can be, for the same blocking voltage, at least an order of magnitude smaller (due to a smaller base thickness and hence shorter time of flight of carriers with the saturated velocity). Also, the use of SiC devices enables the dimensions and masses of pulse devices to be significantly decreased and their operation reliability to be enhanced owing to higher frequencies, a higher junction temperature, and a simpler cooling system.

4.3.1 Design of 4H-SiC SRDD. In the early 2000s, we were the first to discover the phenomenon of subnanosecond interruption of current in $\mathrm{p^+-p_0-n^+}$-type mesa-epitaxial 4H-SiC diodes after they are pumped with a quasiconstant current [70]. Figure 31 shows characteristic processes of recovery of the $\mathrm{p^+-n_0-n^+}$ and $\mathrm{p^+-p_0-n^+}$ diodes after switching from the forward direction to the reverse one. We can see that after attaining a reverse current of 0.6 A, the n-base diodes exhibit a rather soft recovery, which continues for about 16 ns, while p-base diodes recover in a quite different way. The maximum reverse current for the same values of the forward pumping current and reverse voltage was significantly larger, about 1 A, and sharply ended in less than 1 ns. The effect of various factors that determine the character of recovery of the blocking capacity of silicon-carbide diodes with the blocking p-base was theoretically analyzed later in [71]. The initial hypothesis regarding the dominance of the drift mechanism that operates due to the big difference between the mobility of electrons and holes in silicon carbide has been confirmed.

In discussing practical implementation of pulse generators based on diodes with the $\mathrm{p^+-p_0-n^+}$(substrate) structure, the following disadvantages should be noted: deep etching of mesas is needed (across the entire $\mathrm{p_0}$-base thickness) to prevent short-circuiting the $\mathrm{p_0-n^+}$ junction; the creation of an effective protection system to prevent edge breakdown is a very challenging problem; and the operation rate is decreased due to the low mobility of majority carriers (holes) in the blocking $\mathrm{p_0}$-type base.

More promising for high-voltage 4H-SiC SRDDs is the $\mathrm{p^+-p-n_0-n^+}$(substrate) structure that we proposed in [72], where the plasma buildup area and the blocking area are

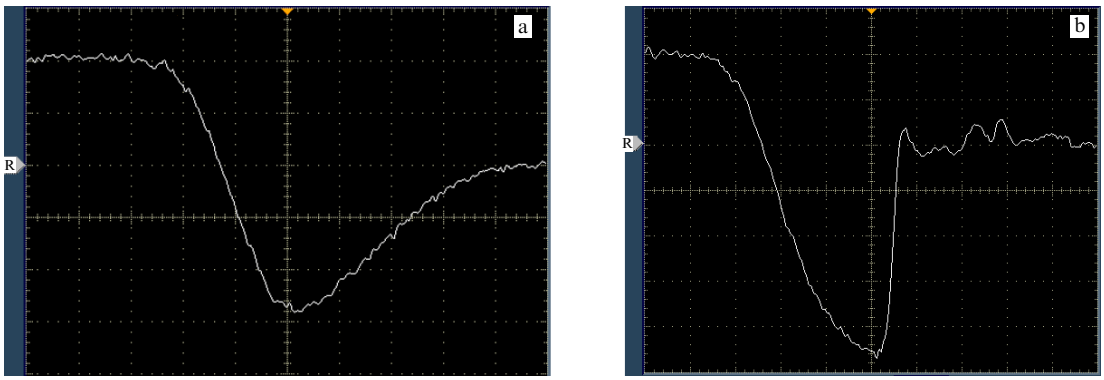

Figure 31. Oscillograms of currents in the process of switching (a) a $p^+-n_0-n^+$ diode and (b) a $p^+-p_0-n^+$ diode from the forward direction to the reverse direction. Vertical scale: 0.2 A per graduation line; horizontal scale: 4 ns per graduation line. Forward current 0.4 A. The zero current level is indicated with an R.

Table 3. Calculated parameters of a two-kilovolt 4H-SiC generator.

Parameter	Value
Pulse amplitude, V	2000
Interrupted current, A	40
Donor density in n-base, 10^{16} cm^{-3}	1.2
n-base thickness, μm	1.3
Diode area, mm^2	0.1
Pulse rise time, ns	0.11

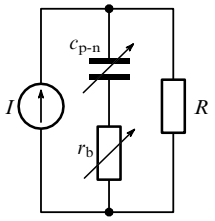

Figure 32. Equivalent circuit of a generator at the stage of interruption by a reverse-current diode: I is the source of quasiconstant current supported by an accumulating inductance (not shown in the circuit); $c_{p\text{-}n}(t)$ and $r_b(t)$ are instantaneous values of the barrier capacity of the p–n junction and the series resistance of the quasineutral part of the base; and R is the load resistance (all calculations were done for $R = 50$ Ω).

separated: the moderately doped p-layer operates as a 'plasma reservoir' (nonequilibrium carriers are pumped into it by a short forward-current pulse), and the lightly doped n_0-layer as the blocking base (the p_0 layer in the $p^+-p_0-n^+$ structure is concurrently the plasma reservoir and the blocking base). No deep etching is needed in the $p^+-p-n_0-n^+$ structure; an efficient protection system can be formed; and the operation rate is supposed to be higher owing to the higher mobility of electrons than of holes.

4.3.2 Analytic models that describe operations of 4H-SiC SRDD with the $p^+-p-n_0-n^+$ structure. In [73], we developed a simple analytic model that describes the operation of generators containing 4H-SiC SRDDs with the $p^+-p-n_0-n^+$ structure. The model was used to theoretically estimate the maximum attainable electrical parameters of high-voltage pulse generators designed on the basis of individual diodes. Table 3 displays the parameters calculated for a two-kilovolt generator.

The calculated duration of the current-interruption phase (leading-edge time of the output pulse with a 2 kV amplitude) is 0.11 ns. To attain an operation rate this high, plasma must be pumped out quite rapidly: the estimated ratio of the pulse leading-edge time and the duration of pumping is approximately 1:10.

The simulation in [73] was limited to an analysis of diodes where the nonlinear electric resistance of the quasineutral part of the blocking n_0-base is negligible compared to the resistance of load at all stages of device operation. We took the effect of the nonlinear electric resistance of the quasineutral part of the blocking n_0-base on the transient process into consideration in [74]. We showed that the parameters of generated pulses strongly affect the shape of the field dependence of the electron drift velocity in 4H-SiC along the hexagonal axis c.

Characteristics of the drift of electrons and holes in 4H-SiC are very different. In [75], we simulated the generation of pulses by a silicon-carbide SRDD with a blocking base of n- and p-types to compare their operation rates. It was assumed in the analysis that the diode does not contain nonequilibrium carriers at the instant when SCA starts expanding (at $t = 0$), and the current that flows through the diode is the initial bias current that recharges the barrier capacity of the p–n junction. An equivalent circuit of the generator at the instant when the current is interrupted by the diode is shown in Fig. 32. The density of the reverse current $j_{p\text{–}n}(0)$ interrupted by the diode at $t = 0$ is chosen to be large enough to minimize the p–n junction area S and hence the barrier capacity $c_{p\text{–}n}$. But if $j_{p\text{–}n}(0)$ increases and S decreases, the resistance $r_b(0)$ increases. The large value of $r_b(0)$ results, in turn, in the emergence of a so-called pedestal, the initial voltage $u(0)$, on the output pulse:

$$u(0) = IR\frac{r_b(0)}{R + r_b(0)}\,. \tag{4.12}$$

If $r_b(0) \sim R$, $u(0)$ can constitute a significant part of the total amplitude of the output pulse ($U = IR$), an effect that is undesirable (and frequently impermissible) from the perspective of practical use of generators. The simulation goal was to calculate time parameters of such generators that ensure a given amplitude of output pulses with a pedestal that makes up no more than 5% of the amplitude. Equation (4.12) shows that if $R = 50$ Ω and $k = u(0)/U = 0.05$, the resistance $r_b(0)$ should be

$$r_b(0) = \frac{k}{1-k}\,R \approx kR = 2.5\ \Omega. \tag{4.13}$$

The following widely used approximation of the dependence of the carrier drift velocity v on the electric field E was used in calculations:

$$v = \frac{\mu E}{\left[1 + (\mu E / v_s)^{\gamma}\right]^{1/\gamma}}, \tag{4.14}$$

where μ is the low-field mobility of the carriers, v_s is the saturated drift velocity of the carriers, and γ is a dimensionless parameter.

In [76, 77], we studied the drift of electrons in n-type 4H-SiC (in the direction of the hexagonal axis c of the crystal) in fields whose strength is 4×10^5 V cm^{-1}. We derived a semiempirical dependence of the electron drift velocity v_n on the field E (see Eqn (4.14)). If the level of doping with donors is $\sim 10^{15}$ cm^{-3}, the parameters are as follows: the low-field mobility of electrons $\mu_n = 950$ cm^2 V^{-1} s^{-1}, the saturated drift velocity $v_{sn} = 1.55 \times 10^7$ cm s^{-1} (the saturated velocity proved to be close to the value obtained by Monte Carlo simulation [78]), and the dimensionless parameter $\gamma_n = 1.15$.

Reliable experimental data on the parameters listed above for p-type 4H-SiC are still missing (transport of hot holes in 4H-SiC has been studied by Monte Carlo simulation [79]). An approximation of the theoretical dependence of v_p on E reported in [79] yielded the following values of the parameters: $\mu_p = 70$ cm^2 V^{-1} s^{-1}, $v_{sp} = 5.9 \times 10^6$ cm s^{-1}, and $\gamma_p = 1.18$.

With Eqn (4.14), the resistance $r_b(0)$ is calculated as

$$r_b(0) = r_{b0}\left[1 + \left(\frac{\mu k U}{L_b v_s}\right)^{\gamma}\right]^{1/\gamma}, \tag{4.15}$$

where $r_{b0} = \rho L_b / S$ is the ohmic-base resistance ($\rho = qn\mu$ is the specific base resistance, q is the elementary charge, n is the density of free carriers in the base, and L_b is the base thickness).

The following initial conditions were chosen for calculations:

(1) the amplitude of the output pulse on the load is close to the diode breakdown voltage. The efficiency of the protection system in high-voltage 4H-SiC diodes is usually such that the maximum reverse voltage does not exceed 90% of the theoretical breakdown voltage U_{br} of a quasi-one-dimensional junction:

$$U = 0.9 U_{br}; \tag{4.16}$$

(2) the base thickness is equal to that of the SCA under the reverse voltage equal to U_{br},

$$L_b = \sqrt{\frac{2\varepsilon U_{br}}{qN}}, \tag{4.17}$$

where $\varepsilon = 8.85 \times 10^{-13}$ F cm^{-1} is the dielectric permittivity of 4H-SiC and N is density of impurities in the blocking base.

Under these conditions, the voltage U_{br} and the density N are related by the equation

$$U_{br} = \frac{\varepsilon E_{br}^2}{2qN}, \tag{4.18}$$

where E_{br} is the critical field strength of the avalanche breakdown of 4H-SiC. The value of E_{br} is related to the density of impurities N in the blocking base by an empirical relation [6]

$$E_{br}[\text{V cm}^{-1}] = \frac{2.49 \times 10^6}{1 - 0.25 \log\left(10^{-16} N\,[\text{cm}^{-3}]\right)}. \tag{4.19}$$

Equations (4.18) and (4.19) can be used to (numerically) calculate the density N for a given voltage U. The diode base thickness L_b can in turn be calculated using Eqn (4.17).

A distinctive feature of p-type 4H-SiC is incomplete ionization of acceptors (aluminum) at room temperature due to the relatively large energy of their ionization: $E_A = 0.19$ eV. (The donors (nitrogen) in 4H-SiC, whose ionization energy is about 0.05 eV, are virtually fully ionized at room temperature.)

Due to the incomplete ionization of acceptors and a relatively low hole mobility, the area of p-base diodes should apparently be larger than that of n-type diodes (for a fixed output-pulse amplitude).

The density of electrons in n-base diodes was assumed to be equal to the density of donors ($n_n = N_d$), while the density of holes in p-base diodes was calculated using the standard neutrality equation

$$n_p = N_v \exp\left(-\frac{E_F}{k_B T}\right) = \frac{N_A}{1 + 2\exp\left[(E_A - E_F)/k_B T\right]}, \tag{4.20}$$

where N_v is the effective density of states in the 4H-SiC valence band, $k_B T$ is the thermal energy, and E_F is the position of the Fermi level in the p-4H-SiC bandgap relative to the upper edge of the valence band.

Using the parameters that were introduced and calculated above, the required junction area S can be calculated as

$$S = \frac{L_b}{qn\mu}\frac{1}{kR}\left[1 + \left(\frac{\mu k U}{L_b v_s}\right)^{\gamma}\right]^{1/\gamma}. \tag{4.21}$$

In accordance with the diagrammatic circuit shown in Fig. 32, the instantaneous voltage $u_{p-n}(t)$ is described by the differential equation

$$u_{p-n} + c_{p-n}\frac{du_{p-n}}{dt}(R + r_b) = U. \tag{4.22}$$

The nonlinear capacitance $c_{p-n}(t)$ in Eqn (4.22) decreases with time due to the SCA expansion into the base. The nonlinear resistance $r_b(t)$ is maximal at the beginning of the current interruption stage and decreases with time due to both the SCA expansion and the weakening of the effect of carrier velocity saturation. The initial condition for Eqn (4.22) is $u_{p-n}(0) = 0$. The terms c_{p-n} and r_b in Eqn (4.22) can be expressed in terms of the voltage u_{p-n} and its time derivative du_{p-n}/dt as follows:

- the capacitance c_{p-n} as a function of the voltage u_{p-n}:

$$c_{p-n} = S\sqrt{\frac{q\varepsilon N}{2(u_{p-n} + U_{bi})}}, \tag{4.23}$$

where U_{bi} is the diffusion difference between potentials at the p–n junction;

- the resistance of the quasineutral part of the base:

$$r_b = \frac{\rho w_b}{S}\left[1 + \left(\frac{\mu u_r}{w_b v_s}\right)^{\gamma}\right]^{1/\gamma}; \tag{4.24}$$

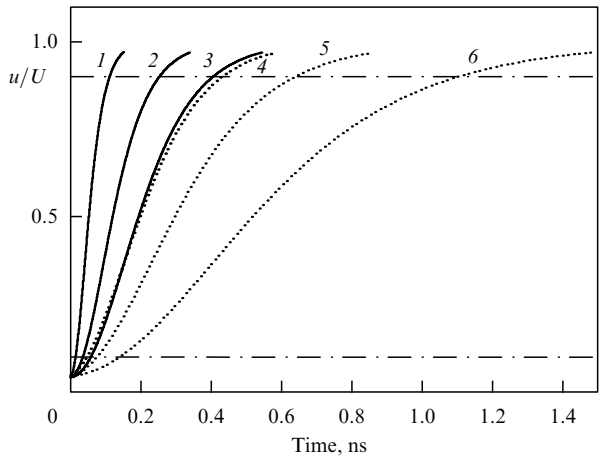

Figure 33. Time dependence of the output voltage calculated for various values of U. Solid curves are for the n-type base and broken curves for the p-type base. Curves *1* and *6*: $U = 1000$ V, curve *2*: $U = 2000$ V, curve *3*: $U = 3000$ V, curve *4*: $U = 300$ V, and curve *5*: $U = 500$ V.

• the voltage decrease on the quasineutral part of the base and its thickness:

$$u_r = U_m - u_{p-n} - Rc_{p-n}\frac{du_{p-n}}{dt}\,, \quad w_b = L_b - \frac{\varepsilon S}{c_{p-n}}\,. \quad (4.25)$$

The sought form of the output pulse, i.e., the dependence $u(t) = u_{p-n}(t) + u_r(t)$, was determined using a combination of numerical methods, including numerical solution of first-order differential equations and numerical solution of transcendent algebraic equations.

Figure 33 shows time dependences of the output voltage calculated for various amplitudes U. We can see that at the amplitude $U = 1000$ V, the pulse rise time (from 0.1 to 0.9) in the case of an n-base diode is about 0.1 ns, while the pulse rise time for a p-base diode is almost 10 times larger. The n-base diodes can generate 3000 V pulses whose pulse rise time is about 0.3 ns. The p-base diodes with the same operation speed can only generate pulses whose amplitude is 300 V. Thus, if the output pulse amplitude and the initial 'pedestal' are fixed, the operation speed of 4H-SiC SRDDs with the blocking p-type base should be much inferior to that of n-type SRDDs. This is due to the lower mobility and density of holes (for the same doping level) and the saturated velocity of their drift.

4.3.3 Experimental 4H-SiC SRDDs. Diodes were crafted in [80] using a commercial n-type 4H-SiC plate with a $p^+-p-n_0-n^+$ structure grown on it. The thickness of the p^+ layer was 2 μm, the density of acceptors in it was $\sim 10^{19}$ cm^{-3}; the p-layer was 5 μm thick, and the density of acceptors in it was 5×10^{16} cm^{-3}; the n_0 layer was 40 μm thick, and the density of donors in it was 1.5×10^{15} cm^{-3}; and the n^+ layer was 1 μm thick, and the density of donors in it was $\sim 1 \times 10^{18}$ cm^{-3}.

The pulse modes of pumping the plasma in and out in the case of 4H-SiC SRDD with the $p^+-p-n_0-n^+$ structure are as follows: (1) pumping should be performed by short pulses (of the order of 10 ns) of forward current; during the pulse time, the nonequilibrium holes injected from a p^+ emitter pass, due to diffusion and drift, a distance not longer than the p-layer thickness; (2) pumping out should be performed by a reverse current pulse that rises even faster, in several nanoseconds. To ensure such regimes for testing diodes, a double-circuit electric setup was designed in which the launch times of the pumping-in and pumping-out pulses were synchronized (Fig. 34).

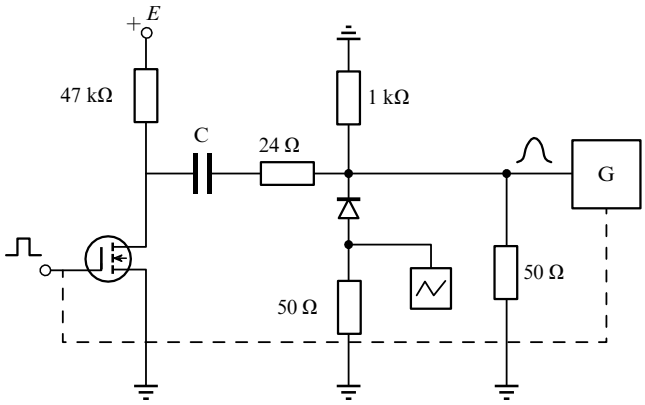

Figure 34. Pulse test circuit.

The pumping circuit was designed as a relaxation generator where a fast-operating silicon 600 V MOS (metal–oxide–semiconductor) transistor SPD02N60C3 with a drain current rise time of 3 ns was used as a normally closed switching element. Forward-current pulses about 10 ns in duration were generated by discharging capacitor C via an open transistor, the diode under testing, and the load resistance $R = 50$ Ω. The amplitude and times of current rise and fall in the pumping circuit are determined by the power source voltage E, the transistor turn-on time, and the capacity of the capacitance C. These parameters can be varied to control the amplitude I_p and duration t_p of the pumping current pulse, i.e., the pumped-in charge of minority carriers Q_p. The pumping-out circuit is designed using a generator, G, of high-voltage pulses in which output pulses are generated by silicon SRDDs. The generator makes outputs under 50 Ω load pulses with an amplitude V_G of up to 5 kV and duration of 4 ns (rise and fall time is about 2 ns). Reverse-voltage pulses are applied with a certain (controllable) time delay with respect to forward-current pulses. The maximum possible rate of the reverse-current rise in the pumping-out circuit is determined by the generator. Oscillograms of the voltage on the load resistance connected in series with the diode (actually, the current that passes through the diode) were recorded using a Tektronix DPO4104 digital oscilloscope with a 1 GHz transmission band.

Pulse testing of 4H-SiC diodes was performed in various modes that differed in the amplitude and duration of forward-current pulses, the amplitude of reverse-voltage pulses, and the time delay of pumping-out pulses with respect to pumping-in pulses. The pulses were repeated with a frequency of 1 Hz. If the shapes of the reverse-current pulses in various circuit operation modes had to be compared, oscillograms were recorded in such a way that the initial segments of reverse current rise coincided in time.

The effect of a subnanosecond interruption of reverse current supported by preliminary injected carriers is illustrated with the oscillograms shown in Fig. 35. Curve *1* shows an oscillogram of the current during operation of a two-circuit setup connected to a resistive load of 50 Ω. The current pulse amplitude in the pumping circuit is 2 A, the

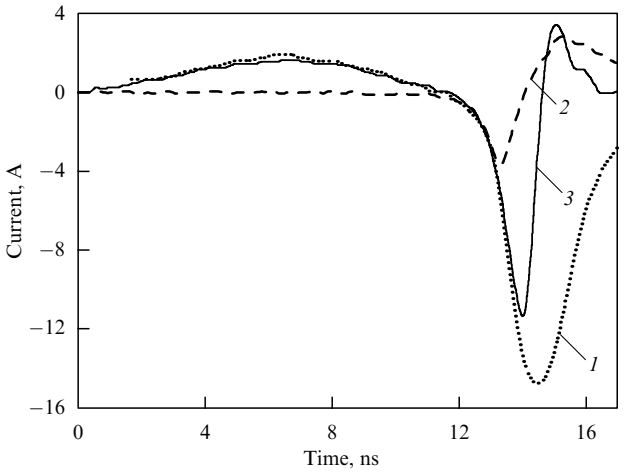

Figure 35. Oscillograms showing the effect of subnanosecond interruption of current.

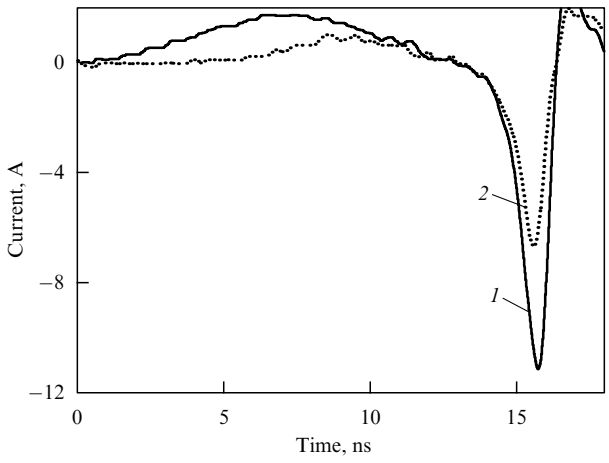

Figure 37. Oscillograms showing the effect of the Q_p value.

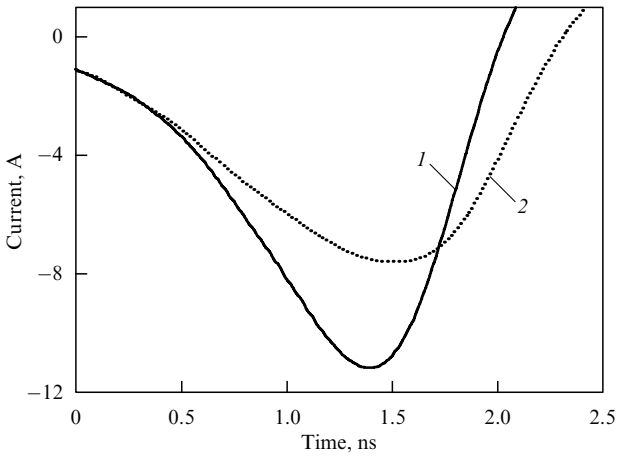

Figure 36. Oscillograms showing the effect of the V_G value.

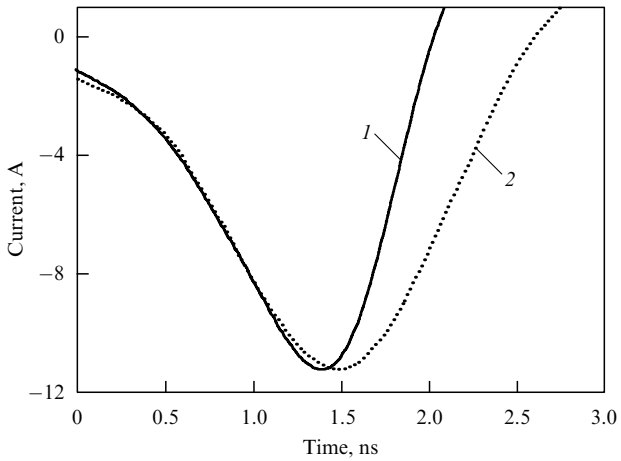

Figure 38. Oscillograms showing the effect of the t_p value.

duration 10 ns, and the current amplitude in the pumping-out circuit is 15 A and duration 4 ns. Curves *2* and *3* display oscillograms of the current for a diode connected in series with the load. Curve *2* shows the blocking capacity of the diode in the pulse mode (with a disconnected pumping circuit). We can see that a capacitive current pulse passes through the diode whose amplitude and duration (4 A and 2 ns) are significantly (several times) smaller than those of the pulse if the circuit is connected to a purely resistive load. Curve *3* shows the SRDD effect: a rise and subnanosecond fall in the reverse current after preliminary pumping in the electron–hole plasma by a forward-current pulse (time of delay of the reverse pulse with respect to the forward pulse was chosen such that the reverse-current amplitude I_m was maximal). The process parameters are as follows: the forward-current pulse amplitude $I_p = 2$ A, the duration $t_p = 10$ ns, the interrupted reverse current $I_m = 11$ A, and the interruption time $t_f = 0.4$ ns.

Figure 36 shows how V_G affects the amplitude and rate of the reverse-current rise and fall. Curve *1* in Fig. 36 reproduces curve *3* in Fig. 35 ($V_G = 750$ V). Curve *2* is recorded at $V_G = 450$ V. We can see that as V_G decreases, the interrupted current I_m also decreases, while its rise time t_e increases. This result is explained by the charge of injected carriers ($Q_e \sim I_m t_e$) pumped out by the reverse current remaining unchanged. If V_G decreases, not only the current rise rate but also the fall rate decrease.

Figure 37 shows how the value of the pumped charge Q_p affects the amplitude I_m. It can be seen that as Q_p decreases (owing to a reduction in I_p and t_p), the interrupted current I_m also decreases. This is explained by the equality of the pumped-in and pumped-out charges of the injected carriers ($Q_p = Q_e$) if the recombination of nonequilibrium carriers in the process of pumping-in and pumping-out can be disregarded.

For a 4H-SiC SRDD with the $p^+ - p - n_0 - n^+$ structure to operate correctly, the pumping duration t_p must be such that within that time, the holes injected from a p^+ emitter can pass, due to diffusion and drift transport, a distance approximately equal to the p-layer thickness. If the time t_p is significantly exceeded, nonequilibrium carriers build up not only in the p-region but also in the blocking n_0-base. We can expect that recovery of the $p - n_0$ junction at the stage of reverse-current interruption would be slower, because it would begin in the presence of nonequilibrium carriers in the n_0-base.

Figure 38 shows how the value of t_p affects the reverse-current interruption rate under otherwise equal conditions. Curve *1* in Fig. 38 reproduces curve *3* in Fig. 35 ($t_p \approx 10$ ns). Curve *2* is recorded at $t_p \approx 100$ ns. The value of I_p is chosen such that the interrupted reverse current I_m remains

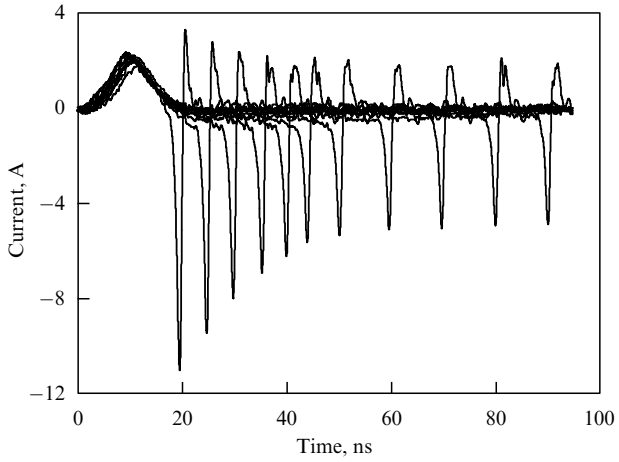

Figure 39. Oscillograms showing the effect of the t_d value.

unchanged. We can see that if t_p increases, the current fall rate decreases in accordance with expectations.

One of the conditions of effective SRDD operation is that the lifetime of nonequilibrium carriers τ be large enough for their recombination during pumping-in and pumping-out to be negligible. It is apparent that if the reverse pulse is delayed with respect to the forward pulse end, the SRDD effect should gradually weaken and fully disappear at $t_d > 3\tau$. Figure 39 shows how the value of t_d affects the reverse-current amplitude. As t_d increases, I_m monotonically decreases, eventually tending to the capacitive current amplitude (cf. curve *2* in Fig. 35). It can be seen that the estimated lifetime of nonequilibrium carriers in the p-layer is $\tau \sim 10$ ns by the order of magnitude.

High-voltage (1600 V) 4H-SiC SRDDs with a record-setting response time (150 ps) were presented in [81]. The diodes were made based on an n-type 4H-SiC plate with the $p^{++}-p^{+}-p-n_0-n^{+}$ structure grown on it. The p^{++} and p^{+}-layers are 0.5 μm thick, and the respective density of acceptors in these layers is 2×10^{19} and 5×10^{18} cm^{-3}; the p-layer is 6 μm thick, and the density of acceptors is 5×10^{16} cm^{-3}; the n_0-layer is 20 μm thick, and the density of donors is 5×10^{15} cm^{-3}; and the n^{+}-layer is 5 μm thick, and the density of donors is 1×10^{18} cm^{-3}. Diodes are 0.8 mm in diameter.

The crafted diode chips were tested as part of a special pulse circuit (Fig. 40). In this circuit, the diode is pumped in by a pulse current source that consists of a source of positive (constant) voltage (V_1), an accumulating capacitor (C_1), charging resistors (R_1 and R_2), and a fast-operating silicon *n*-channel MOS transistor (T). The diode under test (DOT) is included in the discharging circuit of the accumulating capacitor. The capacitor C_1 is charged in the initial state to the source voltage V_1. If the transistor is switched on by a positive gate pulse (V_G), a forward-current pulse flows through the diode, with the amplitude and duration determined by the voltage V_1, the transistor operation time T, and the time of the capacitor C_1 discharge via the transistor, the 50 Ω coaxial cable, and a forward-biased diode.

The amplitude of the forward-current pulses was up to 10 A, and their duration varied in the range 10–20 ns. Plasma was pumped out by a reverse-current pulse using a V_2 pulse generator, whose role was performed by a standard generator manufactured by FID-tekhnika. The generator makes outputs to 50 Ω load positive pulses with an amplitude of up to 5 kV, the duration of about 4 ns, and the leading-edge rise

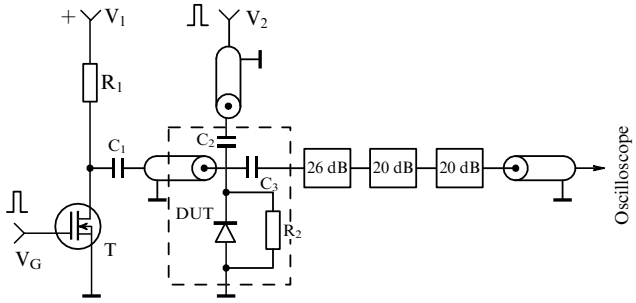

Figure 40. Circuit for pulse testing of diodes. Broken-line rectangle shows the circuit elements included in the microstrip transmission line.

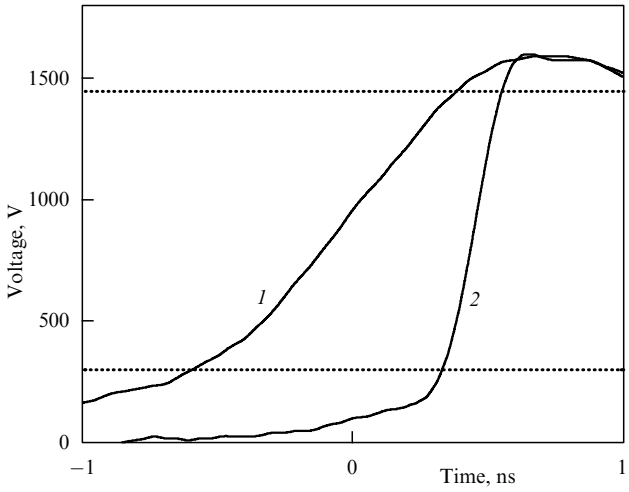

Figure 41. Oscillograms of output pulses: curve *1* is for the disconnected diode, curve *2* for the connected diode.

time of about 2 ns. The input reverse-voltage pulse is sent from the generator to the diode via the 50 Ω line, and the decoupling capacitor C_2 at the instant when the pumping pulse ends. The recording circuit includes a decoupling capacitor C_3, high-frequency attenuators manufactured by Barth Electronics, and a Tektronix DPO70404C digital oscilloscope. The input resistance of the attenuators performs as a 50 Ω load connected in parallel with the diode.

Figure 41 shows oscillograms of the output pulses. Curve *1* is recorded when the diode is disconnected, and therefore the shape of this curve reproduces that of the input pulse (the amplitude 1600 V and the leading-edge rise time about 2 ns). Curve *2* is recorded when the diode is connected. Because the diode is operating under ideal pumping conditions, the leading-edge of the input pulse becomes steeper: prior to the current interruption, the long line is shunted at the end by the small resistance of the diode, and immediately after the blocking capacity of the diode has been recovered, the generator starts outputting to a balanced load of 50 Ω.

The oscillogram of the output pulse (curve *2* in Fig. 41) contains a segment where the voltage increases relatively slowly; this is the so-called pedestal, whose value can be as large as 200 V. The output voltage rapidly increases to 1600 V immediately after the pedestal. The rise time in the rapid growth segment (a 1500 V surge) is 220 ps. The input pulse thus becomes steeper by a factor of 10. This time is apparently determined not by the diode operation speed alone but also by the transmission band of the recording circuit, including a

microstrip line (MSL) and digital oscilloscope (20 GHZ attenuators do not cause any distortions). The rise time of the MSL transient response is 120 ps. The rise time of the transient response of the oscilloscope with a 4 GHz transmission band is 90 ps. Given these values, the calculated time of current being interrupted by the diode is 150 ps. To the best of our knowledge, this time is the smallest among high-voltage (over 1000 V) silicon-carbide circuit breakers.

5. Simulating transient processes in 4H-SiC-based power bipolar devices

Simulations of processes that occur in power bipolar devices are an integral and mandatory part of designing and studying such devices. Simulations not only enable an analysis of experimental results, but also often prompt ideas for new experiments. In addition, a proper simulation not infrequently 'saves' researchers from carrying out experiments that are complicated and labor-consuming but are doomed to failure.

In this section, we present results of simulations of transient processes in power bipolar devices based on 4H-SiC: thyristors, bipolar transistors, and diodes. We also consider phenomena that are common to all silicon-carbide-based devices: electron–hole scattering, the efficient emitter problem, and fundamental physical restrictions on the maximum blocking voltage and the maximum current densities [69].

5.1 Thyristors

The first thyristor (dinistor) based on silicon-carbide was presented at the Ioffe Institute in 1988 [82, 83]. The blocking voltage of this device was 30 to 50 V, and the effective area was 7×10^{-4} cm^2. Spectacular progress was attained in subsequent years in increasing the blocking voltage, the working area, and the current switched by SiC thyristors [84]. An 18-kilovolt-class SiC thyristor has been developed to date [85, 86]. Thyristors based on 4H-SiC with a blocking voltage of 9 kV, a large current rise rate dI/dt, and the switched pulse current up to $\sim$ 5500 A have been studied in [87].

The main physical properties of SiC thyristors were studied in the late 20th and early 21st centuries after thyristor structures had appeared whose blocking voltage was several hundred volts. When structures with a high blocking voltage $V_b \geqslant 3$ kV appeared, it was shown that a conceptually new turn-on mechanism can be realized in high-voltage SiC transistors, in addition to the turn-on mechanism characteristic of the analyzed in-depth silicon-based thyristor [93].

5.1.1 Turn-on process. The main specific feature of the turn-on process in SiC thyristors — a temperature dependence of the current rise rate in the turn-on process that is 'anomalous' compared with similar dependences in Si and GaAs thyristors — was experimentally discovered in [94, 95]. The turn-on time in Si and GaAs thyristors increases as the temperature grows due to the reduced mobility, the diffusion coefficient, and the carrier saturation rate. The mobility, the diffusion coefficient, and the carrier saturation rate in SiC also decrease as the temperature grows. Nevertheless, the SiC thyristor turn-on time decreases as the temperature grows, and, as follows from Fig. 42, this decrease is rather significant. The temperature dependence of the turn-on time at $T \geqslant 380$ K tends to saturation. If the thyristor is cooled, the turn-on time constant rapidly increases. For example, the turn-on time constant at $T = 160$ K is approximately 30 times larger than at $T = 500$ K [88].

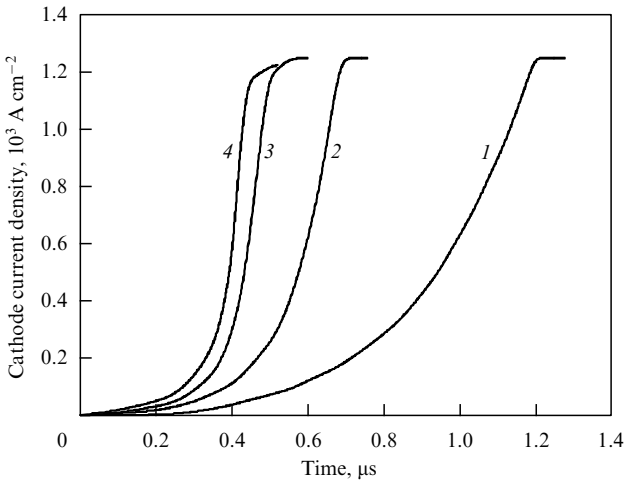

Figure 42. Time dependence of the current in the process of turning on a thyristor with a blocking voltage of 2.6 kV at various temperatures: 293 K (curve *1*), 330 K (curve *2*), 379 K (curve *3*), and 404 K (curve *4*). The cathode voltage is $V_c = 200$ V, and the load resistance is $R_l = 50\ \Omega$.

This phenomenon was explained in qualitative terms in [95]. The effect is due to the ionization energy of the shallowest acceptor level in 4H-SiC (aluminum) being rather large (~ 0.2 eV). Therefore, only 1–2% of Al atoms are ionized at room temperature ($N_A \sim (1-2) \times 10^{19}$ cm^{-3}) in the heavily doped p^+-emitter of the 'constituent' p^+-n-p^0 transistor. As the temperature grows, the hole density in the emitter increases. Consequently, the injection coefficient of the p^+-emitter and hence the gain factor of the 'constituent' p^+-n-p^0 transistor increases. The explanation proposed in [95] is based on an equation derived in [96],

$$\tau_r = 2\left(\frac{\tau_1\tau_2}{\alpha_1+\alpha_2-1}\right)^{1/2}, \tag{5.1}$$

where τ_r is the time constant of current rise, τ_1 and τ_2 are the times of flight of minor carriers through the thyristor bases, $\alpha_1 = \gamma_1\alpha_{T1}$ and $\alpha_2 = \gamma_2\alpha_{T2}$ are the respective gain factors of the constituent transistors in the thyristor structure (the upper p^+-n-p^0 and the lower $n-p^0-n^+$), γ_1 and γ_2 are the injection coefficients of the upper p^+-n and lower n^+-p emitter-base junctions, and α_{T1} and α_{T2} are the respective transfer coefficients for the upper (narrow) and lower (blocking) base.

According to [95], τ_r decreases as the temperature grows as a result of an increase in α_1. But this interpretation is intrinsically inconsistent: Eqn (5.1) was derived in [96] under the assumption that injection coefficients of both junctions, γ_1 and γ_2, are equal to unity. Consequently, Eqn (5) can be used to compare thyristors with different values of α_T, but it is not suitable for analyzing the actual situation where the injection coefficient γ_1 changes as the temperature varies.

An adequate analytic study and a computer-aided analysis of the turn-on process accelerating as the temperature increases were reported in [97, 98]. An expression for τ_r was derived in [97] based on the charge control model under the condition of a low injection level in the blocking base of the thyristor. For the most important case where $\alpha_1+\alpha_2 = \gamma_1\alpha_{T1} + \gamma_2\alpha_{T2} \Rightarrow 1+\delta$ and $\delta \ll 1$, the expression for τ_r has the form

$$\tau_r = \frac{(1-\gamma_1\alpha_{T1})\tau_1 + (1-\gamma_2\alpha_{T2})\tau_2}{\gamma_1\alpha_{T1}+\gamma_2\alpha_{T2}-1}, \tag{5.2}$$

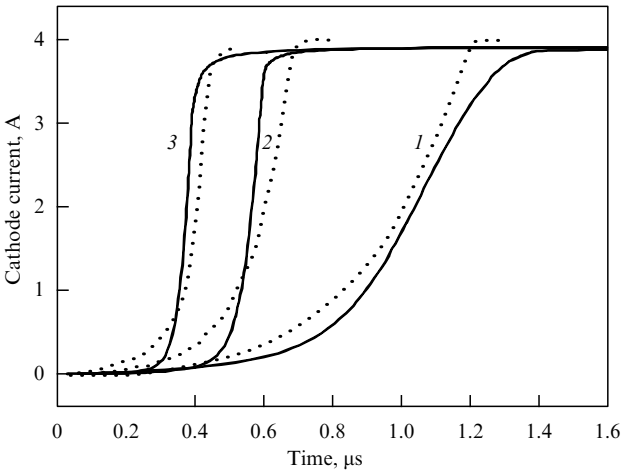

Figure 43. Time dependence of current in the process of turning on a thyristor with a blocking voltage of 2.6 kV at a temperature of 293 K (curve *1*), 330 K (curve *2*), and 379 K (curve *3*). Solid curves show experimental data, and dotted curves simulation results.

where τ_1 and τ_2 are the respective lifetimes in the thin and blocking base of the thyristor. If the temperature dependence of the hole density in a heavily doped emitter and the main parameters of the thyristor are known, Eqn (5.2) can be used to assess the temperature dependence of τ_r. However, for the comparison of experimental data with theoretical results to be correct, the temperature dependence of not only γ_1 but also other thyristor parameters must be taken into account. Apart from this, it is of importance to take nonlinear effects also affecting the temperature dependence of τ_r into account. Such calculations are only possible as part of numerical simulations.

The Issledovanie (Research) software package [99] was used in [97]. This computer program is based on transport equations for charge carriers that enable a correct account of the entire set of nonlinear effects for high injection and high doping levels, including Auger recombination, electron–hole scattering, bandgap narrowing, and the dependence of kinetic coefficients and the lifetime of charge carriers on the doping level in heavily doped structure layers [100].

Figure 43, where numerical results are compared with experimental data, shows a very good agreement between simulation results and experiment.

The analytic results obtained in [97] were used in [101] to analytically estimate the turn-on rate in the cases of low and high injection levels in the blocking base of a thyristor that correspond to the low and high density of the current flowing through the thyristor after it is turned on. It was shown that the turn-on time constants can be very different in the considered cases. The ratio of the turn-on times for the low (τ_{rL}) and high (τ_{rH}) injection levels can be as high as several dozen: $\tau_{rL}/\tau_{rH} \geqslant 20$. The analytic estimates obtained are confirmed by numerical results.

It was noted in [92, 102, 103] that SiC thyristors are turned on by a rather large gate current. The turn-on occurs in the blocking base of the thyristor, not at low injection levels, as is the case with 'classical' Si thyristors, but at a level that is intermediate between low and high injection levels. Reasons for this phenomenon have been analyzed in [104], leading to the conclusion that a turn-on mechanism qualitatively different from that of classical Si thyristors is realized in high-voltage thyristors at room and lower temperatures. Analytic estimates for the new turn-on mechanism have been obtained, and temperature characteristics of thyristors and turn-on parameters as functions of the blocking voltage have been explored as part of computer simulations using the Issledovanie software package. A conclusion of importance for practice has been made: to obtain SiC thyristors with reproducible parameters and the required resilience to the dV/dt effect, an external shunting of the base–emitter junction in the thin base of the thyristor is needed.

5.1.2 Turn-off process. The thyristor turn-off by the control gate reverse current in SiC thyristor structures with a relatively low blocking voltage at room temperature has been studied in [105–107]. The turn-off of the thyristor with a blocking voltage of 2.6 kV in the temperature range 293–500 K has been analyzed in detail in [108].

The maximum current that can be turned off by the control gate reverse current is limited by a breakdown of the low-voltage control junction. Another way of turning off 4H-SiC thyristors was studied in [91]: pulse short-circuiting of the control junction can be used for that purpose. The current turned off by the external control signal can be significantly increased in this case. A silicon MOS transistor was used to do so in [91], whose resistance in the open state is of the order of 1 Ω. It was shown that to have the thyristor completely turned off, the duration of the pulse that short-circuits the control gate must exceed some threshold Δt^*_{off}. Otherwise, after the pulse ends, the thyristor spontaneously turns on again. It is qualitatively clear that Δt^*_{off} is the time interval during which the charge of the carriers injected into the thyristor bases decreases to a value that is smaller than the critical turn-on charge. Because the lifetime in the blocking base of the thyristor increases as the temperature grows [109], Δt^*_{off} also increases with temperature. The temperature dependence of Δt^*_{off} is similar to that of the lifetime. This turn-on regime has been studied in detail using the Issledovanie software package in [110].

Figure 44 displays the results of simulations of the turn-off process by means of a pulse ohmic short-circuiting control junction by an MOS transistor. Corresponding experimental data are shown in the inset [91]. Good agreement between experimental and theoretical results can be seen. The simulation enabled clarification of the nature of a long 'delay' between the end of the short-circuiting pulse and the beginning of current rise in the spontaneous turn-on process (curve *3* in Fig. 44). As follows from Fig. 44, the duration of this 'delay' significantly exceeds both the current rise time in the turn-on process and the thyristor turn-off time.

The delay time is typically indicative of the time during which the nonequilibrium charge equal to the critical turn-on charge is built up. But because a thyristor spontaneously turns on if $\Delta t_{off} < \Delta t^*_{off}$, it is clear that the charge contained in the bases after the end of the short-circuiting pulse exceeds the critical value. The simulation showed that the turn-on process begins immediately after the short-circuiting pulse ends, without any delay. However, prior to the current attaining a certain value, the turn-on occurs at a low injection level. As was noted above, the turn-on time constant at a low injection level τ_{rL} can be significantly larger than the τ_{rH} constant at a high injection level. In the case shown in Fig. 44, $\tau_{rL}/\tau_{rH} \approx 16$.

5.1.3 Critical turn-on charge and the dV/dt effect. The concept of critical charge was formulated in [111] and further

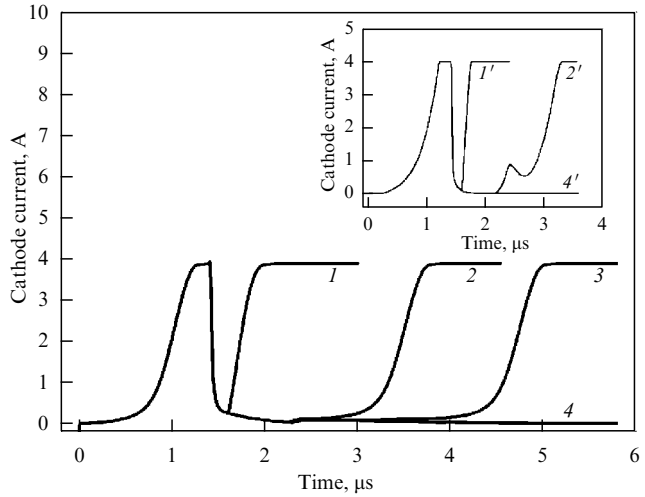

Figure 44. Calculated time dependences for various durations of a short-circuiting pulse Δt_{off}. Similarly to experiment [91], the anode-control gate junction was short-circuited with a resistance of 1 Ω at the instant $t = 1.4$ μs. Δt_{off} values: *1* — 0.2 μs, *2* — 0.8 μs, *3* — 0.82 μs, and *4* — 0.83 μs ($\Delta t_{\text{off}} > \Delta t^*_{\text{off}}$). The inset shows corresponding experimental dependences [9]. $T = 300$ K. Blocking voltage $V_0 = 200$ V, load resistance $R_1 = 50$ Ω. Δt_{off}: *1′* — 0.2 μs, *2′* — 0.8 μs, *4′* — 0.9 μs ($\Delta t_{\text{off}} > \Delta t^*_{\text{off}}$).

developed in [112, 113]. This concept enables an analysis from a single perspective of both the pulse processes that occur when a thyristor is turned on due to dV/dt, by short control pulses, by short light pulses, etc., and 'slow', quasi-stationary turn-on processes. The set of these processes includes turning on by a slowly rising control current, temperature change, a quasistationary increase in the anode voltage, etc.

The critical charge density in silicon thyristors ranges from $\sim 10^{13}$ cm^{-3} in specially designed devices with very low n_{cr} values and extremely low turn-on control currents [114, 115] to $(2-3) \times 10^{16}$ cm^{-3} in powerful high-voltage thyristors. Similar values of n_{cr} are characteristic of GaAs thyristors [116].

The critical charge density in SiC thyristors was for the first time determined in [89] for relatively low-voltage structures with a blocking voltage ~ 400 V. The main characteristics of the critical charge in high-voltage structures with a blocking voltage of 1.5–2.6 kV were studied in [92, 102]. It was shown in [92] that n_{cr} is of the order of 10^{16} cm^{-3} in 2.6 kV SiC thyristors at room temperature, and this density monotonically decreases as the temperature grows. The density is $n_{\text{cr}} \approx 10^{14}$ cm^{-3} at $T = 500$ K.

A simulation performed using the Issledovanie package found a qualitative disagreement with the model in [112, 113] that describes critical charge parameters in SiC thyristors. The root of this disagreement was studied by analytic and numerical methods in [102]. It was noted that several factors must be taken into account in studying the critical charge in SiC thyristors. First, the injection coefficient γ_1 for the emitter — a thin, heavily doped base junction — is assumed to be unity in theory [112, 113]. While this assumption is fulfilled with a high accuracy for silicon thyristors, it fails for SiC structures: due to the large ionization energy of the acceptor level (Al) in the p-emitter, the γ_1 value at room temperature is noticeably less than unity [97]. The second important difference distinguishing silicon-carbide thyristors from silicon ones is that SiC structures are turned on at an injection level intermediate between the low and high levels of injection to the blocking base of the thyristor rather than at a low level. It is clear that if the thyristor cannot be turned on at a low injection level; an additional critical charge must be accumulated to turn it on at an intermediate injection level. It is expected that a significant role is played by the current dependence of the transport coefficient α_{T2} in the blocking base of thyristor.

The voltage that can be applied to a thyristor decreases as the voltage rise rate increases (the dV/dt effect). This effect has been thoroughly studied in Si and GaAs thyristors [116–120]. The dV/dt effect is of special importance for SiC thyristors because it is believed that one of the main advantages of SiC devices is their ability to operate in very-high-frequency circuits [121].

The dV/dt effect in high-voltage SiC thyristors was studied in [122, 123]. If the duration Δt of the leading edge of the voltage pulse applied to a thyristor is less than the time of flight of minor carriers through the thin base of the thyristor, as a result of which the carriers do not have enough time to recombine during the leading-edge rise time, the minor carrier charge $Q = \int_{V_{\text{bi}}}^{V_0} C(V)\, dV$ emerges in each device base if the voltage V_0 is applied. Here, $C(V)$ is the capacitance of the junction per unit area and $V_{\text{bi}} \sim 3$ is a built-in potential. Thus, having determined the minimal voltage under which the thyristor can be turned on by a pulse with a sufficiently steep leading edge, we can directly determine the critical-charge density of the device.

Pulses with a leading-edge time of 30 ns were used in [122, 123] to turn on the thyristor using the dV/dt effect. Figure 45 shows time dependences of voltage on the thyristor at various temperatures. For each temperature, the voltage amplitude V_0 corresponds to a minimal value that turns on the thyristor. We can see that the higher the temperature, the smaller voltage is needed to turn on the thyristor.

Temperature dependences of the minimal voltage V_0 that were calculated using the Issledovanie software package are compared in Fig. 46 with experimental data. The plot shows that although the calculated and measured results agree in qualitative terms, their quantitative disagreement is rather significant. It is shown that if an agreement between the calculated and experimental results can be attained at room temperature by varying lifetime values in thyristor

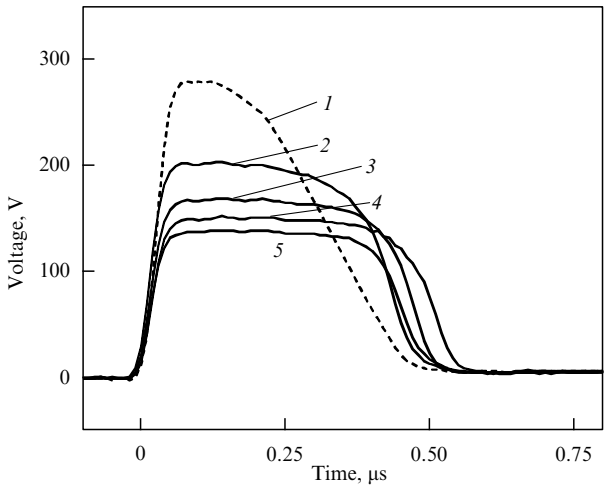

Figure 45. Time dependences of voltage on a 1.5 kV thyristor at various temperatures: *1* — 300 K, *2* — 344 K, *3* — 392 K, *4* — 442 K, and *5* — 504 K. The pulse rise time is 30 ns. The voltage amplitude V_0 corresponds for each temperature to the minimum value that turns on the thyristor.

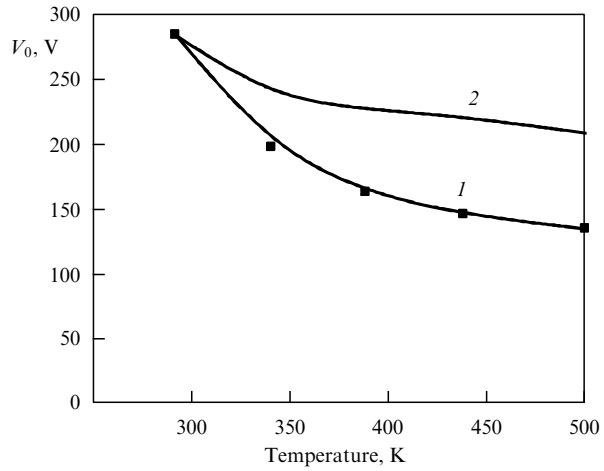

Figure 46. Temperature dependence of the amplitude V_0. *1* — experimental data, *2* — calculation results obtained in a one-dimensional model using the Issledovanie software package.

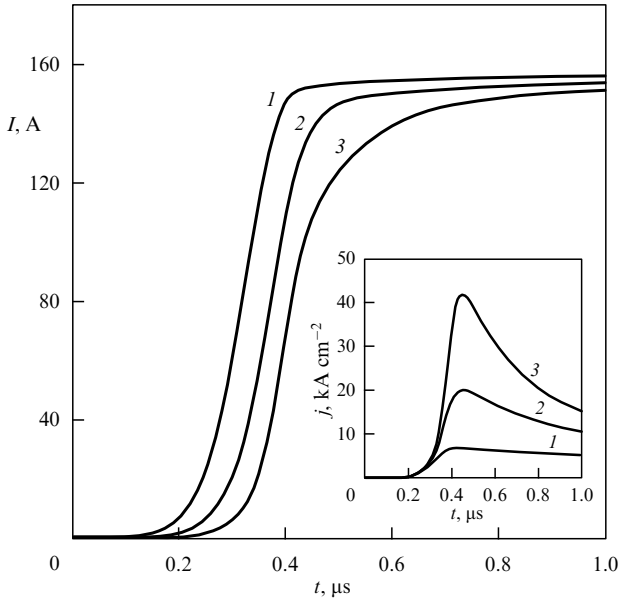

Figure 47. Time dependence of current in turning on an optothyristor at various values of the optical window radius r_0: *1* — 800 μm, *2* — 400 μm, and *3* — 200 μm. The inset shows the corresponding time dependence of the current density.

bases, the experimental dependence $V_0(T)$ cannot be satisfactorily described within a *one-dimensional* approach under any reasonable assumptions.

The approach proposed in monograph [123] was used in [122] to develop a quasi-two-dimensional model that enabled a very accurate description of the experimental dependence $V_0(T)$ using the Issledovanie package. Good agreement between the calculated and experimental data on the current rise rates in the turn-on process has also been obtained within the same quasi-two-dimensional approach.

5.1.4 Optothyristors. Semiconductor devices based on Si and GaAs that are switched by light pulses [124] are used in numerous applications intended for synchronization of power laser devices, excimer laser power units, and implementation of electrically insulated high-voltage power circuits (see, e.g., [125–127]). Optical turn-on of an SiC thyristor was presented for the first time at the Ioffe Institute [128]. Later, in [129], the potential was demonstrated to turn on a SiC thyristor using an ultraviolet (UV) LED. A high-voltage (12 kV class) SiC optothyristor was turned on using a UV laser with a wavelength of 266 nm to a 100 A current, and the process was studied in [130]. The thyristor turn-on time was 10–20 ns for an optical pulse time of 25–30 ps and the pulse energy $J \approx 10$ μJ.

A model of turn-on and propagation of the turned-on state in an SiC optothyristor was developed based on the adiabatic approximation in [131] using the Issledovanie package. The model enabled assessing the area initially turned on by light, the thyristor turn-on time constant as a function of the energy of the UV source used for switching, and the structure overheating with consideration for the switched current $I_{\max}$ (Fig. 47). Figure 47 shows that although the turned-on state propagates in a spontaneous way, if the optical window size is chosen incorrectly, the current density in the device being turned on can exceed 40 kA cm^{-2}. The overheating of the active area in the structure being turned on can be higher than 2000 °C.

A characteristic of SiC optothyristors is the so-called axially symmetric configuration: the device is turned on by light in a circular window of a small radius r_0, and the turned-on state then propagates in a spontaneous way to the entire area of the device [122, 123]. Specific features of the turn-on process determined by such a configuration of actual devices were studied analytically and numerically in [134–136].

Propagation of the turned-on state was studied in [134] using a numerical model and an analytic approach. A surprising result was obtained and correctly interpreted: it was shown that at the initial propagation stage whose duration is $\sim (2-3)\tau$ (where τ is the thyristor turn-on time constant), the propagation speed is relatively small, especially in the axially symmetric case. It was believed previously that the propagation speed increases as the current rise rate in the turned-on part of thyristor increases (to become saturated at a very large current density.) The result obtained should be taken into account in choosing the permissible current rises rate $\mathrm{d}I/\mathrm{d}t$.

Specific features of the stationary distribution of carriers and the character of retaining current in the axially symmetric case were analyzed in [135]. The relative contribution of field and diffusion mechanisms of turned-on state propagation was analyzed. It was shown that if the initial carrier density $p_l(0)$ is sufficiently large (proportional to the current to which the thyristor is connected), the area occupied by the turned-on state expands as $p_l(0)$ increases. This result, which always holds in the planar case, was believed to be universally correct. It was shown, however, that in the axially symmetric case, when the initial carrier density is relatively small (the current is close to the retaining current), the carrier density in the stationary case is larger than the initial density $p_l(0)$. Figure 48 shows that if the initial current density (the initial $p_l(0)$ value) is small, the stationary-state current density in the center of the optical window increases compared to the initial one. This effect should be taken into account in turning on SiC optothyristors for currents close to retaining currents.

Relations between the critical charge density, the retaining current, and the maximum current density have been analyzed in the axially symmetric case in [136].

Transient processes in superhigh-voltage optothyristors with a blocking voltage of 18 kV were explored experimentally in [137, 138]. The amperage of the switched current in

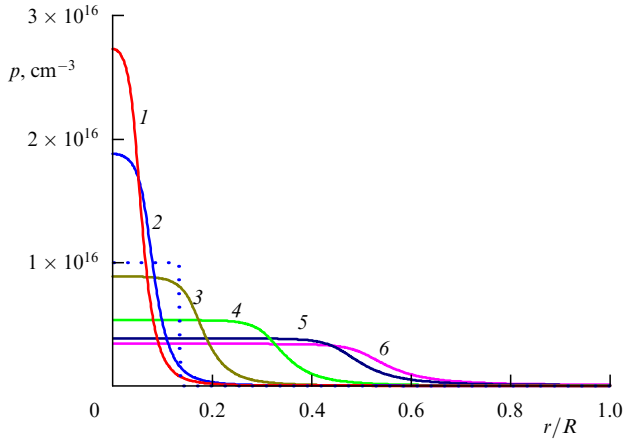

Figure 48. Stationary profiles of the distribution of holes $p(r)$ in an axially symmetric case for various initial values $p_l(0)$: *1* — 0.08×10^{17} cm^{-3}, *2* — 0.10×10^{17} cm^{-3}, *3* — 0.20×10^{17} cm^{-3}, *4* — 0.40×10^{17} cm^{-3}, *5* — 0.60×10^{17} cm^{-3}, and *6* — 0.65×10^{17} cm^{-3}. The current density at each point is proportional to p. The dotted line shows the initial distribution of holes $p_l(0)$ for curve *2*.

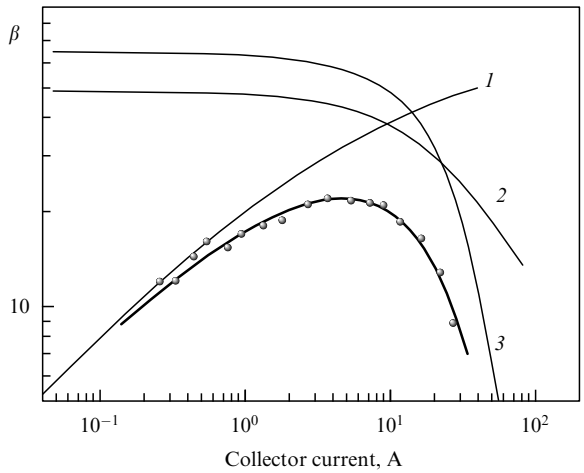

Figure 49. Gain factor β of 4H-SiC-BT as a function of the collector current. $T = 293$ K. Dots show experimental data for the collector-base voltage $V_{CB} = 100$ V. The bold curve shows results of calculations in a semi-empirical model [67]. Thin curves represent the contribution of recombination in the space charge area (curve *1*), surface recombination (curve *2*), and recombination in the emitter (curve *3*).

operations with a purely inductive load was as high as 1200 A (for an energy of the triggering light pulse ~ 40 μJ and its duration 30 ps). If such a thyristor is turned on for relatively small currents $\leqslant 20$ A, the turn-on process exhibits an unusual 'two-step' behavior. The current rises at the first turn-on stage with a characteristic time constant of 15–20 ns. Having attained an intermediate maximum, the current begins decreasing with a significantly larger time constant, this decrease being followed by a new increase in the current to a stationary value determined by the voltage on the device and the load resistance. This effect has never been observed in thyristors with a blocking voltage of 12 kV. A comprehensive explanation of the two-stage turn-on phenomenon was given in [139] on the basis of calculations with the Issledovanie package.

5.2 Bipolar transistors

Relatively high-voltage power bipolar transistors (BTs) based on 4H-SiC with a blocking voltage $V_b \geqslant 1.5$ kV and an acceptable gain factor in the common-emitter circuit $\beta \sim 30$ appeared in the early 21st century [140–142]. Power silicon-carbide-based BTs are currently considered to be very promising fast-operating switching devices owing to a combination of properties such as a high blocking voltage, a low on-resistance (R_{ON}), and a quite large gain factor. 4H-SiC BTs have been developed whose blocking voltage exceeds 9 kV [143], with a gain factor in the common-emitter circuit $\beta > 300$ [144], and with rather low R_{ON} values [145].

Transient characteristics of 4H-SiC BTs (with $V_b = 1.8$ kV) were studied for the first time in [64]. It was shown that an important role is played in BT turn-on by surface recombination, and this role is significantly enhanced as the current is squeezed out to the emitter edges (crowding).

One of the BT parameters that is most important for operations in the active mode is the gain factor in the common-emitter circuit β. The dependence of β on the collector current in high-voltage 4H-SiC and the factors that limit the value of β were studied in [146, 147]. Figure 49 shows β as a function of the collector current that is typical for 4H-SiC BTs [148]. The gain factor increases in the region of small currents, attains a maximum, and then decreases as the current grows further. As follows from Fig. 49, results of calculations in a semi-empirical model [148] agree well with experimental data. In addition to the recombination of nonequilibrium carriers in the BT base, the model incorporates contributions from recombination in the area of the emitter-base space charge, recombination in the emitter, and surface recombination. The decrease in the local gain factor β towards the emitter center under conditions of crowding is also taken into consideration. The model developed was successfully used to interpret the experimental dependence of the gain factor β on the collector current in the temperature range 300–520 K [147].

While the gain factor in the common-emitter circuit, β, is the most important parameter if a BT is used in the active mode, one of the most important parameters of the BT used as a high-power switch is the open-state resistance R_{ON}. This parameter is in most cases equal to (or even greater than) the resistance of the unmodulated collector layer of high-power BTs [149, 150]. Several studies have shown, however, that R_{ON} can be significantly reduced by modulating the collector layer resistance with minor carriers injected from the base layer in the saturation mode [151, 152].

The main physical features of modulation of the collector resistance were studied in [153] using the effective one-dimensional model developed at the Ioffe Institute [154]. This model was successfully used to describe Si- and GaAs-BTs also in modes of maximum high current densities [155, 156].

An accurate quantitative description of transient processes in high-power SiC BTs with an interdigitated structure requires two-dimensional (2D) simulation in general. However, the main physical regularities of the BT turn-on and turn-off processes can often be conveniently examined within one-dimensional models. Simulation of this kind enables a transparent analysis of the effect of the main parameters of the structure and switching modes on transient processes.

The simulation in [153] shows that modulation by minor carriers can greatly reduce the BT resistance in the turned-on state (Fig. 50). Figure 50 shows that if the input signal I_b is sufficiently strong, the transistor resistance can be reduced, owing to collector-layer modulation, to values that are

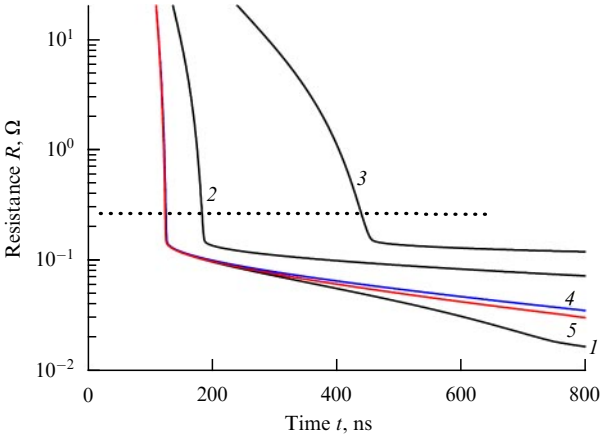

Figure 50. Time dependence of a BT in the process of turning on. Results calculated for a BT with the parameter characteristic of a BT with a blocking voltage of 1200 V. Curves *1–3* are calculated for the lifetime in the base $\tau_b = 100$ ns and the lifetime in the collector $\tau_c = 2$ μs. The base current is $I_b = 0.6$ A (curve *1*), 0.2 A (curve *2*), and 0.06 A (curve *3*). Curve *4*: $I_b = 0.6$ A, $\tau_b = 20$ ns, and $\tau_c = 2$ μs. Curve *5*: $I_b = 0.6$ A, $\tau_b = 100$ ns, and $\tau_c = 400$ ns. The dotted straight line shows the resistance of the unmodulated collector layer.

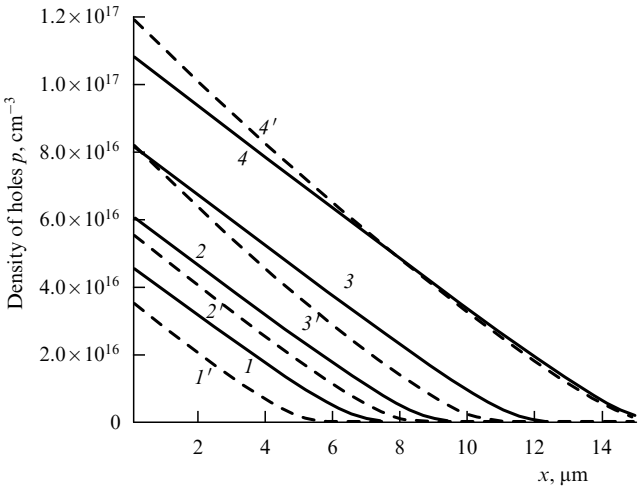

Figure 51. Distribution of holes $p(x)$ along the collector of a BT with parameters characteristic of a BT with a blocking voltage of 1200 V at various time instants. The transistor switches at the instant $t = 0$ to the saturation mode, and holes begin diffusing in the direction opposite to the field, thus reducing the collector resistance. The base current is $I_b = 0.2$ A (curves *1*, *1′* and *2*, *2′*) and $I_b = 0.6$ A (curves *3*, *3′* and *4*, *4′*). Time $t = 300$ ns (curves *1*, *1′* and *3*, *3′*) and $t = 600$ ns (curves *2*, *2′* and *4*, *4′*). Solid curves *1–4* represent results of an analytic calculation, and broken curves *1′–4′* results of calculations in a numerical model [153].

significantly smaller than the resistance of the unmodulated collector. It was shown in [153] that the effective modulation of the collector resistance is possible if the transistor is turned on sufficiently fast, this requirement being fulfilled if the turning-on base current has a large amplitude and steep leading-edge rise.

An analytic model of BT collector layer modulation was developed in [157] on the basis of a theory of minor-carrier diffusion in the direction opposite to the electric field vector at a high injection level [158]. The model in [157] allows calculating the carrier distribution and the collector modulation level in the stationary state and, in addition, tracking minor carrier (hole) motion along the n-type collector layer in the process of modulation (Fig. 51).

The slowest process in bipolar devices that determines the maximum operation frequency of the devices is turning-off. If the current density in high-power switching BTs increases in the open state, the turn-on time decreases, while the turn-off time, on the contrary, increases. It is clear, however, that a buildup of minor carriers in the collector in the process of collector modulation and a reduction in its resistance can significantly increase the delay time and the transistor turn-off time [80]. This can make the required reduction in R_{ON} at high-frequency switching unacceptable.

It was shown experimentally in [159, 160] that the delay and turn-off times can be significantly reduced if a reverse base current pulse is applied in the process of turning off [161]. Conditions for turning off Si BTs under effective modulation of the device collector with minor carriers were studied in [162] using the model in [153]. The turn-off process was explored in both the 'standard' mode, where the base current is turned off, and the mode of turning off by a negative base current. It was shown that for quite realistic values of the turning-off base current, the turn-off time can be reduced by a factor of ~ 40 compared to the turn-off time at zero base current. The delay time can also be significantly reduced (Fig. 52).

Figure 52 shows that both the delay time and turn-off time monotonically decrease as the negative base current $(-I_b)$ increases. If $I_b = -0.2$ A (Fig. 2b), the delay time is 820 ns,

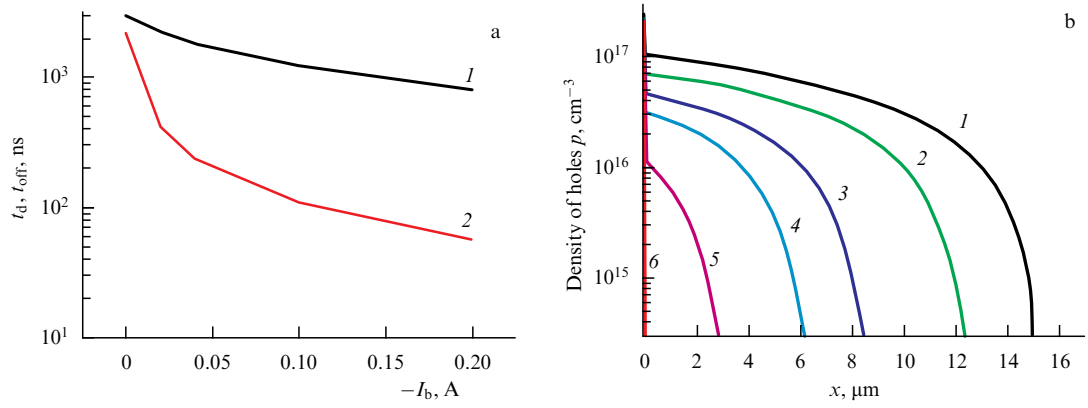

Figure 52. (a) Time delay t_d (curve *1*) and turn-off time t_{off} (curve *2*) as a function of the negative (turn-off) base current I_b. (b) Distribution of holes in a collector in the turn-off process at $I_b = -0.2$ A. The turning-off pulse of the base current is applied at the instant $t = 5000$ ns. Curve *1* — 5000 ns, *2* — 5300 ns, *3* — 5600 ns, *4* — 5700 ns, *5* — 5800 ns, and *6* — 5840 ns.

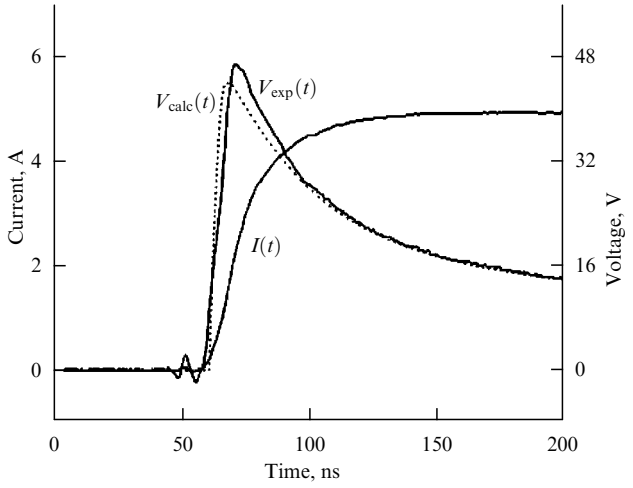

Figure 53. Time dependence of the current and voltage on a 6 kV diode in the turn-on process. Solid curves show experimental oscillograms. The dotted curve represents the results calculated using the Issledovanie software package [165].

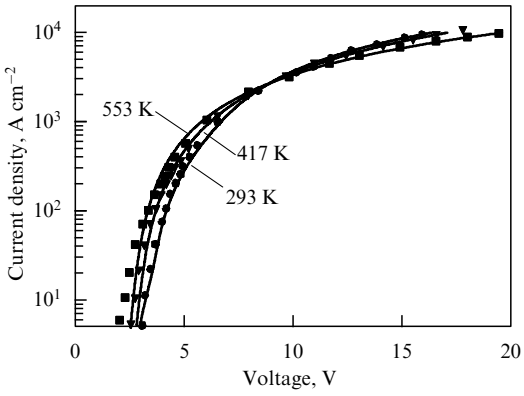

Figure 54. Forward CVCs of a 6 kV 4H-SiC diode. Dots represent experimental data, and solid curves results of calculations with consideration for EHS.

and the turn-off time is 57 ns. If the transistor is turned off at zero base current, the delay time decreases by a factor of 3.6, and the turn-off time by a factor of 38 compared to the corresponding times in the standard mode. The turn-off time is virtually equal to the turn-on time. We note that an experimental study [160] found that if a large negative base current is used to turn off the transistor, the delay time is reduced by a factor of 4, and the turn-off time by a factor of 20.

5.3 Rectifying p–i–n diodes

High-voltage rectifying p–i–n-4H-SiC diodes with an operating voltage of several kilovolts were presented in the early 2000s (see, e.g., [163]). Diodes with the operating voltage ≈ 20 kV and operating current of several hundred amperes were developed shortly afterwards [164].

5.3.1 Turn-on process. The most important parameters in studying turn-on process are modulation of the diode base resistance in transient process and the forward voltage drop on the structure at the end of the transient process in a stationary state.

Figure 53 shows time dependences of the current and voltage on a 6 kV diode in the process of switching [165]. A forward current pulse passed through the diode in the experiment; the pulse amperage increased from zero to 5 A in approximately 30 ns. The $V(t)$ dependence clearly shows two characteristic stages of the switching process. The first corresponds to 'recharging' the emitter–base junction. A voltage surge is observed at this stage, with the amplitude determined by the resistance of the unmodulated base. Afterwards, as carriers accumulate in the base, the voltage decreases to a stationary value that is determined by the resistance of the base modulated by the build-up of minor carriers. The analysis in [165] shows that if the current passing through the diode increases this rapidly, the base can be modulated owing to rapid motion of the electron pulse leading edge with a saturation velocity $\sim 10^7$ cm s^{-1} and a relatively slow motion of the hole pulse leading edge in the opposite direction.

Fast switching of a diode in forward direction was studied in [166, 167] using analytic and numerical methods. It was shown that if the current amplitude is quite large and the rise time short, violated-neutrality modes occur. The diode base can be modulated owing to propagation of fast waves of electrons and holes moving in opposite directions with saturated velocities of charge carriers in a strong electric field.

5.3.2 Lifetime of minor carriers. Interestingly, as late as the mid-1990s it was believed that the lifetime of minor carriers in silicon carbide cannot be large in principle due to a high density (at a level of 10^{20} cm^{-3} or even higher) of stoichiometric defects in the form of excessive silicon. These concerns proved to be unfounded, however, and the goal to increase the lifetime has been successfully achieved. In the mid-2000s the record-setting long lifetime in the n-base of the 4H-SiC diode at room temperature was 1.55 μs, but the lifetime presently observed in thick layers of n-type silicon carbide is several tens of microseconds [169].

The lifetime in the bases of p–i–n diodes is usually determined by measuring either the duration of the high reverse conductivity phase in switching the diode from the conducting state to the blocking state (Lax method [170]) or the rate with which the post-injection electromotive force (EMF) decreases (Gossick method [171]). The results yielded by both methods for silicon diodes are usually very close. However, the Lax method is inapplicable to silicon-carbide structures [100, 172, 173]. The most detailed analysis of the reasons for this situation was performed in [100] on the basis of qualitative arguments and numerical simulations using the Issledovanie package.

A detailed comparison of experimental data and simulation results showed that a very narrow layer with a very small lifetime often emerges in silicon-carbide p–i–n diodes on the emitter-base interface. Such a layer can emerge because high-temperature buildup of a highly doped p-layer results in growth of the number of defects on the emitter–base interface due to a mismatch between the lattice parameters of the highly doped and undoped layers and due to diffusion of admixture Al atoms and self-diffusion. Because of the presence of such a 'damaged' region near the p–n junction, after the diode has been switched from the forward direction to the reverse direction, the space charge area near the SCA junction begins rapidly recovering (the time during which the blocking capacity recovers is controlled by the carrier lifetime in the damaged layer), and hence there is virtually no phase where a constant reverse current flows. We note that the

possible existence of such a damaged layer with a short lifetime can also play an important role in operations of transistor and thyristor structures.

On the other hand, the Gossick method enables an accurate measurement of the lifetime in the bases of SiC-p–i–n diodes in a broad temperature range [172–174].

5.4 Specific features of physical processes in silicon-carbide-based bipolar devices

5.4.1 Electron–hole scattering. SiC devices can operate in pulse modes at current densities of up to 10^5 A cm^{-2} in the mode of short individual pulses [175]. The operational current density in the mode of so-called long pulses (duration 8–10 ms) can be as high as several thousand amperes per cm^2 [176]. Experience in operating Si and GaAs devices shows that electron–hole scattering (EHS) at large current densities can significantly diminish the effective ambipolar mobility of carriers [177, 178].

The first experiments where EHS was studied in silicon carbide were reported in [179]. An original technique was proposed in this study to determine EHS parameters by analyzing pulse isothermal CVCs of 4H-SiC diodes. Figure 54 shows forward CVCs of a 6-kilovolt 4H-SiC diode measured at 293–553 K and the current densities up to $j = 10^4$ A cm^{-2}. We can see that if the current density is sufficiently high, 'inversion' of the CVC temperature dependence occurs. The inversion point corresponds to the current density of the order of 2000–3000 A cm^{-2}. (These values are more than an order of magnitude larger than the inversion current density for similar silicon structures.) A simple semi-empirical model was proposed in [179] that enables the EHS parameters to be determined by analyzing CVCs at large current densities.

The mobility component that is due to EHS is usually described by the formula

$$\mu_{\rm np} = G\,\frac{p_0}{p}\,, \tag{5.3}$$

where p is the hole density and G and p_0 are the characteristic EHS constants [100]. The EHS contribution to the voltage drop on the device base then has the form

$$V_{\rm eh} = \frac{jW}{qGp_0}\,, \tag{5.4}$$

where j is the current density, W is the base thickness, and q is the elementary charge. Experimental CVCs presented in Fig. 54 were used in the semi-empirical model to obtain the value $Gp_0 = 5.8 \times 10^{19}$ V^{-1} cm^{-1} s^{-1}, which is four times smaller than the corresponding value for Si and 60 times smaller than for GaAs. This result implies that EHS in SiC affects ambipolar mobility and the voltage drop on bipolar-device bases much more strongly than in silicon and gallium arsenide devices [180].

A more accurate analysis using the Issledovanie package yielded an estimate of the possible effect of contact resistance on the EHS contribution in the range of relatively small current densities.

We note that the equations describing EHS are incorporated in the most popular advanced packages of commercial simulators such as DESSIS (Device Simulation for Smart Integrated Systems), Atlas, and Medici in a form that does not provide a correct simulation of EHS in bipolar devices [181].

5.4.2 Efficient-emitter problem in SiC-based bipolar devices. Analytic and numerical estimates show that characteristics of bipolar silicon-carbide devices are far from optimal [182]. A reason for this situation is the low injecting capacity of highly doped p^{++}-type emitters. It is such emitters that are used in thyristors, BTs, and SiC-based diodes. As was noted above, the ionization energy of the shallowest acceptor level in 4H-SiC, aluminum, is ~ 0.2 eV. Therefore, only $\sim 2\%$ of Al atoms are ionized at room temperature in the heavily doped ($N_{\rm A} \sim 10^{19}$ cm^{-3}) p^{++}-layer. As a result, the injection coefficient of SiC emitters is much less than unity.

The problem of increasing the injection coefficient of p^{++}-type SiC emitters was studied analytically and numerically in [182] with nonlinear effects such as narrowing of the bandgap with an increase in doping level, Auger recombination, EHS, and radiative and surface recombination taken into account. The analytic study was based on the well-known 'saturation current' $j_{\rm sn}$ model [183] that has been used many times to assess the quality of emitters in Si and GaAs devices. The numerical analysis was performed using the Issledovanie package. It was shown that to improve the injecting capacity of the emitter, a 'damaged layer' must be removed that often emerges on the highly doped p$^+$-emitter–n-base interface (see Section 5.3.2).

Estimates were obtained for an 'ideal' emitter in which the carrier lifetime is controlled only by basic effects, i.e., radiative recombination and Auger recombination. The dependence of $j_{\rm sn}$ on the doping level $N_{\rm a}$ is shown to have its minimum near $N_{\rm a} \approx 4 \times 10^{20}$ cm^{-3}, which corresponds to $j_{\rm sn} \approx 2 \times 10^{-49}$ A cm^{-2}. This $j_{\rm sn}$ value is two orders of magnitude smaller than the smallest $j_{\rm sn}$ observed in SiC-based devices. We note that the minimum observed in the $j_{\rm sn}(N_{\rm a})$ dependence is rather 'flat', such that if $N_{\rm a}$ increases from $N_{\rm a} = (5-6) \times 10^{19}$ cm^{-3} (a value rather frequently used in designing SiC devices) to the optimal value $N_{\rm a} \approx 4 \times 10^{20}$ cm^{-3}, the injecting capacity of emitters does not significantly increase. The main strategy to improve the injection capacity of the emitter is to increase the carrier lifetime [184]. However, if $N_{\rm a}$ decreases to a value $N_{\rm a} \leqslant 1 \times 10^{19}$ cm^{-3}, an acceptable value of the injection coefficient cannot be obtained even if the lifetimes are very large.

5.4.3 Maximum blocking voltage and maximum current densities. State-of-the-art technologies enable the production of structurally perfect layers of n-type 4H-SiC several hundred micrometers thick with a lifetime of carriers in these layers of several dozen microseconds. However, a question arises related to the complexity of emerging production and economic problems: what is the level to which the voltage of an individual SiC device should be reasonably increased?

Silicon-based electronics encountered a similar problem about 30 years ago when the state of the technology in principle enabled the production of unique devices that could operate at a mains frequency of 50 Hz with a blocking voltage $V_{\rm b}$ up to 80 kV. Nevertheless, the $V_{\rm b}$ values in actual silicon-based devices (diodes and thyristors) do not exceed 8–10 kV. A detailed analysis of the level to which the voltage of an individual Si-based device should be reasonably increased was performed in [185] with consideration for all the main nonlinear processes.

A detailed analysis of this problem for SiC-based devices is reported in [186]. The analysis takes into account that the

lifetime of minor carriers in SiC greatly increases as the temperature increases (see Section 5.3.2); the injecting capacity of actual SiC emitter junctions is currently significantly worse than that of emitter junctions in Si structures; and the efficiency of EHS is much higher in silicon carbide than in silicon (see Section 5.4.1).

The following condition was used as a criterion that sets the limit to increasing the blocking capacity of the devices: the V_b value of the structure should be reasonably increased until the forward-voltage drop on the structure in the conducting state exceeds the total of the forward-voltage drops on two structures connected in series that can block the same V_b voltage.

Results of analytic and numerical estimates are presented in [186] as 'level curves' on the (W, τ) plane (where W is the blocking-base thickness and τ is the carrier lifetime in the base). Such curves were plotted in [106] for ambient temperatures equal to 300, 450, 600, and 850 K and operational forward-current densities j_F equal to 150, 300, 700, 1000, and 2000 A cm^{-2}. The level curves for two temperatures and two values of the operational current density are plotted as an example in Fig. 55. Each pair of the selected values of W and τ determines a point on the (W, τ) plane. If this point is located *below* the level curve for the selected j_F value, the forward-voltage drop on an individual device is smaller than on two devices with the base width $W/2$ and the lifetime τ in the base connected in series. But if the selected point lies *above* the corresponding level curve, it is reasonable to use two devices connected in series instead of a single device.

For a rough estimate of the blocking capacity of SiC devices, it is assumed that a device with a 10 μm thick base can block a voltage $V_b \approx 1$ kV. For example, if the value $W = 200$ μm is chosen, the calculation was performed for 20 kV class devices.

Figure 55 shows that the effect of a reduction in the injecting capacity of an emitter can be compensated by an increase in the lifetime of charge carriers in the structure base layer. For example, if $T = 600$ K and $j_F = 1000$ A cm^{-2}, the use of a single device with the base thickness $W = 275$ μm (which corresponds to $V_b \approx 27.5$ kV) and an 'ideal' emitter is justified for the lifetime $\tau = 22$ μs, while if an actual emitter is used, the lifetime should be no less than $\tau = 28$ μs.

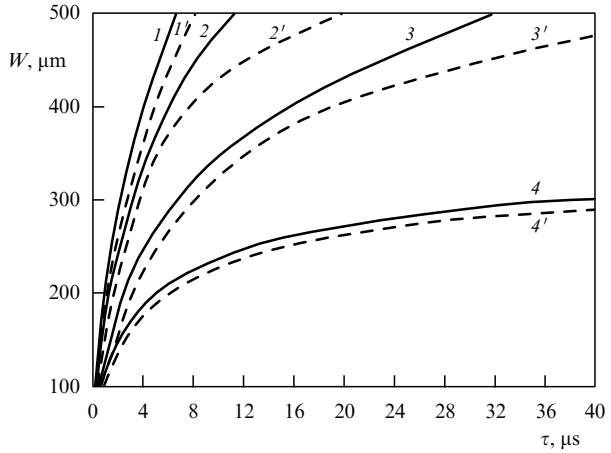

Figure 55. Level lines at the structure temperature $T = 300$ K (curves *1*, *1′* and *2*, *2′*) and $T = 600$ K (curves *3*, *3′* and *4*, *4′*). Solid curves are calculated for an 'ideal' emitter, and broken curves for an 'actual' emitter [173]. Current density j_F: 150 A cm^{-2} (curves *1*, *1′* and *3*, *3′*) and 1000 A cm^{-2} (curves *2*, *2′* and *4*, *4′*).

Three characteristic regimes should be distinguished in discussing the maximum current density in SiC devices. The first extreme case corresponds to self-heating of the device in the direct-current regime. The second (opposite) regime corresponds to device operations in the 'short'-pulse regime. This means a situation where the heat that is released during a pulse does not have enough time to reach the heat sink. To standardize the results and enable their comparison, so-called 8/20 μs industry-standard pulses are used: these are triangle-shaped pulses whose leading-edge time is 8 μs and trailing-edge time is 20 μs. At the same time, to characterize the short-pulse regime, rectangular pulses whose duration is 20–50 μs are infrequently used. Finally, the 'long'-pulse regime corresponds to using rectangular pulses whose duration is equal to a mains-frequency half-period (10 ms for the 50 Hz frequency and 8 ms for the 60 Hz frequency).

Self-heating of SiC devices in the direct-current regime was theoretically and experimentally studied in [187]. It was shown that the isothermal CVC of the devices measured in a broad temperature range can be used as a basis for a valid analysis of operations in the direct-current regime, which is apparently nonisothermal. If an efficient heat sink is available, devices can maintain operability at current densities up to ~ 2000 A cm^{-2}. An N-shaped CVC can occur under certain conditions when the current passing through the device decreases as the bias increases.

The long-pulse regime was theoretically and experimentally analyzed in [176]. It was shown that devices can endure several 8 ms long pulses with the current density amplitude ~ 9000 A cm^{-2}. To correctly describe self-heating in this regime, a thermoelectric model was proposed that is based on preliminarily measured isothermal CVCs. The model provides a good description of the time dependences of self-heating for current densities as high as ~ 5000 A cm^{-2}. Qualitative agreement is observed in the entire range of current densities up to 9000 A cm^{-2}.

Short (20 μs) pulses were used in [175]. The current density attained was ≈ 65 kA cm^{-2}. The temperature of the device was ≈ 1650 K. Repeated application of such pulses or an attempt to exceed the established current density resulted in the destruction of the device. The maximum current density in a single pulse was ~ 100 kA cm^{-2}.

5.5 Conclusions

Although advanced software packages of commercial simulators of semiconductor devices, such as DESSIS, Atlas, and Medici, are now available, the use of independently developed, problem-oriented computer models combined with analytic studies enables identification and analysis of the main physical regularities of the processes that occur in silicon-carbide-based bipolar devices. Using such models and suitable analytic calculations provided a description of all the main processes observed in silicon-carbide-based bipolar devices, including diodes, bipolar transistors, and thyristors.

6. Silicon-carbide-based nanoelectronics

6.1 Spin color centers in silicon carbide as a platform for sensorics, quantum photonics, and environmental information processing

The unique quantum properties of nitrogen-vacancy (NV) color centers in diamond encouraged researchers to seek

those centers with functional quantum properties in silicon carbide that can extend the capacities of such systems [188–205] to new areas. Silicon carbide has now become a flexible and practical platform to be used in modern quantum technologies. The atomic-size color centers in bulk and nanocrystalline SiC are a promising system for spintronics, photonics compatible with fiber optics, quantum processing of information, and environmental sensing.

The options of high-temperature optical spin manipulations with both spin ensembles and individual spins open a new era in the application of spin phenomena in both academic and applied research. Performing quantum operations in living systems, including neural networks, is no longer limited by temperature considerations because all these phenomena occur at room temperature or higher.

SiC was shown to have at least two color center families with $S = 1$ and $S = 3/2$, whose structure is a combination of silicon and carbon vacancies. They have the property of optical alignment of spin-level population and enable manipulation with spin at room temperature. It was found that the ground and excited states in the $S = 3/2$ family have spin $S = 3/2$, and the ground state population can be inverted by means of optical pumping, which results in induced microwave radiation (the maser effect) at room temperature or higher temperatures.

Engineering various types of SiC micro- and nanostructures that contain color centers is arousing increasingly great interest owing to their possible applications in electronic and photonic devices. Based on the successful use of metamaterials with NV centers, we can assume that a similar combination can be proposed for color centers in SiC, whose radiation range extends to the near-IR region (800–1600 nm), a pass-band for fiber optics and living systems.

Spin manipulations have been performed using optical detected magnetic resonance (ODMR), level anti-crossing (LAC), ODMR with 'hole burning' (HB), and cross-relaxation (CR). These operations resulted in changes in spin-level populations, which in turn strongly affected the photoluminescence (PL) intensity of spin centers. Variations in the local field in the vicinity of spin centers can be recorded by optical methods owing to changes in PL intensity in the near-IR region; a distinctive feature of that luminescence is that it falls into the pass-band of fiber optics and living matter.

The spin level energy is calculated using the spin Hamiltonian

$$H = \gamma \mathbf{SB} + D\left[S_z^2 - \frac{1}{3}S(S+1)\right], \qquad (6.1)$$

where $\mathbf{S}$ is the electron spin operator, $\gamma = g\mu_B$ is the gyromagnetic ratio, g is the electron g-factor, μ_B is the Bohr magneton, and D is a parameter that characterizes fine-structure splitting in an axial crystalline field.

Spin color centers are usually denoted by the phononless lines (PLLs) that correspond to them: V1, V2, V3, and V4. Table 4 contains PLL energies on 4H-SiC, 6H-SiC, and 15R-SiC polytypes.

In this review, we discuss experimental accomplishments in magnetometry and thermometry with a micrometer and submicrometer resolution that are based on manipulations with spin states using ODMR, HB, LAC, and CR in a zero or nonzero magnetic field and a broad range of temperatures. A new, fully optical, technology was proposed for magnetometry and thermometry that is based on LAC in the ground and excited states and a fully optical technology for thermometry based on CR of the energy levels in silicon-carbide spin centers. A suite of devices designed to use spin centers in SiC is presented in a series of patents and publications [200, 201, 206–216].

Figure 56 shows a simplified diagram of a scanning device designed as a combination of an ODMR spectrometer and a confocal optical microscope. As the active material, this device uses an SiC crystal that contains spin color centers. The spin centers are created in the crystal by irradiating it with electrons with an energy of 1–2 MeV. Varying the electron flux allows controlling the density of spin centers in a broad range down to discerning individual centers in the light-excited volume; such centers can simultaneously perform as sensors of magnetic fields or temperature, qubits (qudits), and single-photon sources. The maximum possible miniaturization in the elemental base of micro- and optoeletronics means engineering a device based on a single atom, single molecule, or single defect. This sci-fi scenario has started to be realized now, after the unique optical and magnetic properties of the spin centers in diamond and silicon carbide were discovered.

A laser beam in the near-IR range (750–820 nm) is focused on an SiC crystal onto a spot less than 1 μm in diameter to excite the PL of spin centers; the luminesce is recorded by a photodetector (PD) and synchronous detector (SD) at the modulation frequency of a radio frequency oscillator (RFO) or the modulation frequency of the magnetic field. Figure 56 shows the optically induced alignment of spin-level populations in a zero magnetic field at room temperature for spin color centers in SiC crystals of various polytypes. The inverse population of spin levels in a zero magnetic field (maser effect) at room temperature is observed for V2 centers in 6H-SiC and 15R-SiC, V1 and V3 centers in 6H-SiC, and V3 in 15R-SiC. Pulse measurements were conducted using an acoustic optical modulator (AOM) and special hardware and software that generated specified sequences of optical and radio-frequency pulses.

ODMR method and level anti-crossing. As an example, Fig. 57 shows signals of ODMR and level anti-crossing (LAC) of V2 spin centers in a 4H-SiC crystal that were recorded at room temperature using the change in PL intensity of spin centers in the near-IR region (see Fig. 56); the energy of the corresponding spin levels is shown in Fig. 57a for the $\mathbf{B} \| c$ orientation of the magnetic field. Changes in the PL of the spin centers in constant and oscillating low-frequency magnetic fields were recorded by means of synchronous detection.

Table 4. Optical transition energies/wavelengths for PLLs at a temperature of 4 K; fine-structure splitting Δ ($\Delta = 2|D|$) in a zero magnetic field (zero-field splitting: ZFS) at room temperature for a family of spin color centers with $S = 3/2$ in 4H-, 6H-, and 15R SiC. For all centers, $g \approx 2.003$.

Polytype	4H-SiC		6H-SiC			15R-SiC		
PLL	V1	V2	V1	V2	V3	V2	V3	V4
E, eV/nm	1.438/862	1.352/917	1.433/865	1.397/887	1.368/906	1.399/886.5	1.372/904	1.352/917
Δ, MHz/10^{-4} cm^{-1}	39/13	66/22	27/9	128/42.7	27/9	139.2/46.4	11.6/3.87	50.2/16.7

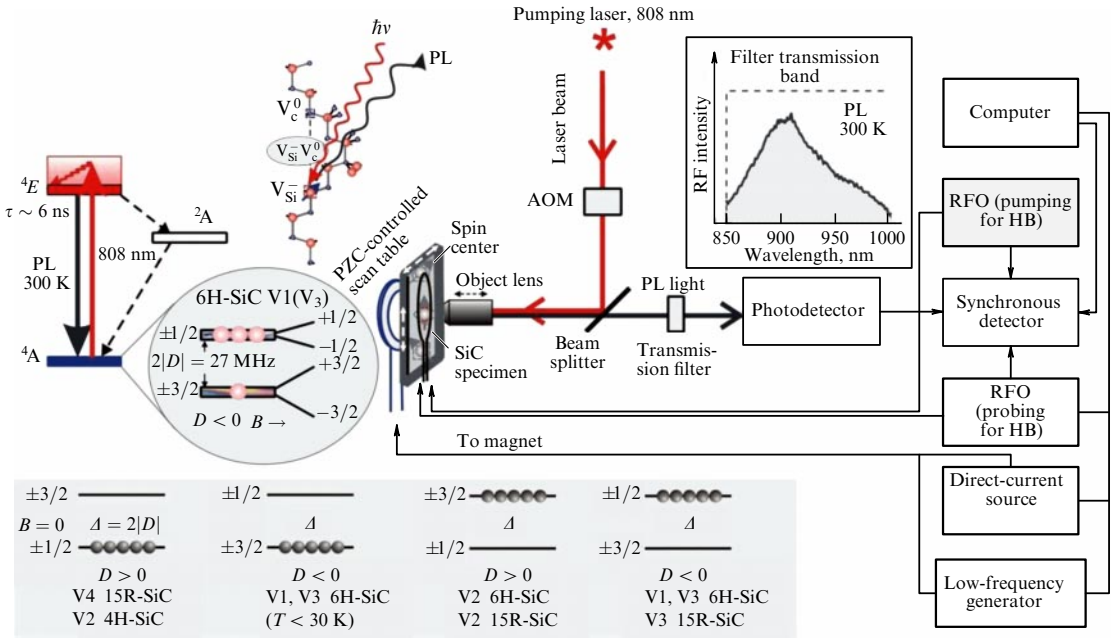

Figure 56. Simplified block diagram of a scanner for measuring magnetic and temperature fields with a submicrometer spatial resolution designed based on a magnetic-resonance spectrometer and confocal microscope. Highlighted in grey are the units of the facility that are used for 'burning holes'. Insets display information on the optical alignment of populations of various spin centers. Notation: PL — photoluminescence, AOM — acoustic optical modulator, RFO — radio-frequency oscillator, PZC — piezoelectric cell, and HB — hole burning.

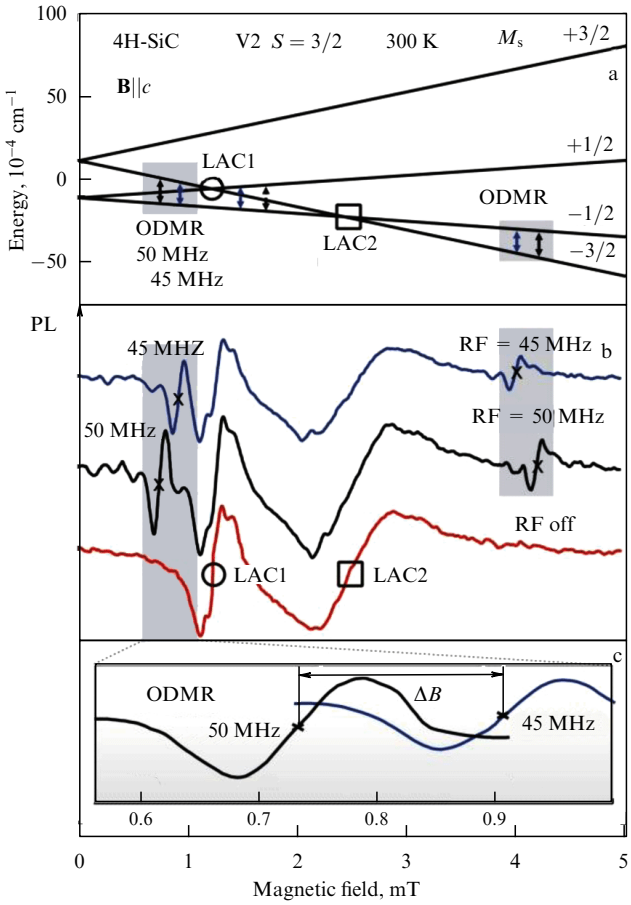

Figure 57. (a) Spin-center energy levels. (b) Signals of anti-crossing of spin levels and ODMR obtained by synchronous detection of changes in PL of the spin center in a 4H-SiC single crystal in a constant magnetic field and an oscillating low-frequency magnetic field. (c) Shift of the ODMR line (enlarged) in a magnetic field for two frequencies.

Displayed are LAC signals in the absence of an RF field (RF turned off), denoted as LAC1 and LAC2, and two ODMR spectra recorded when the RF field is turned on at frequencies of 50 and 45 MHz. This choice of frequencies is explained by the following circumstance: when an ODMR signal comes close to a LAC1 signal, the ODMR signal significantly increases, and its intensity comes close to that of the LAC1 signal, as shown in Fig. 57b. Figure 57c shows the (enlarged) shift of the ODMR line in a magnetic field at frequencies of 50 and 45 MHz, which explains the principle of magnetic field measurements using the ODMR method; the crystal size can be diminished in this method to several dozen micrometers while preserving the high density of spin centers. The magnetic fields for level anti-crossing points are $B_{\mathrm{LAC1}} = D/(g\mu B)$ for levels $M_S = +3/2$, $M_S = +1/2$ and $B_{\mathrm{LAC2}} = 2D/(g\mu B)$ for levels $M_S = -3/2$, $M_S = -1/2$. The LAC1 anti-crossing point is weakly dependent on the orientation of crystals in the magnetic field; it is for this reason that it is used to measure magnetic fields and temperatures in powder materials.

ODMR with '*hole burning*' enables a significant reduction in the width of optical-response lines under synchronous detection and hence a noticeable enhancement of the sensitivity of measurements. These effects are also promising for the development of hardware (qubits and qudits) intended for quantum computations and development of artificial intelligence.

Figure 58a shows results of burning holes in a nonuniformly broadened ODMR line in a 15R-SiC crystal at room temperature; shown in the upper part of the figure are spin-center levels that clarify the HB principle. RF pumping saturates the spin transition $M_S = -1/2 \leftrightarrow M_S = -3/2$ at one particular value of D. Due to spin relaxation, it also affects the transition $M_S = +1/2 \leftrightarrow M_S = +3/2$ with the same D. A satellite should therefore appear at the frequency $f_{s1} = f_p + 2\gamma B$. If the uniform broadening is larger than the Zeeman splitting, the same pumping also saturates the

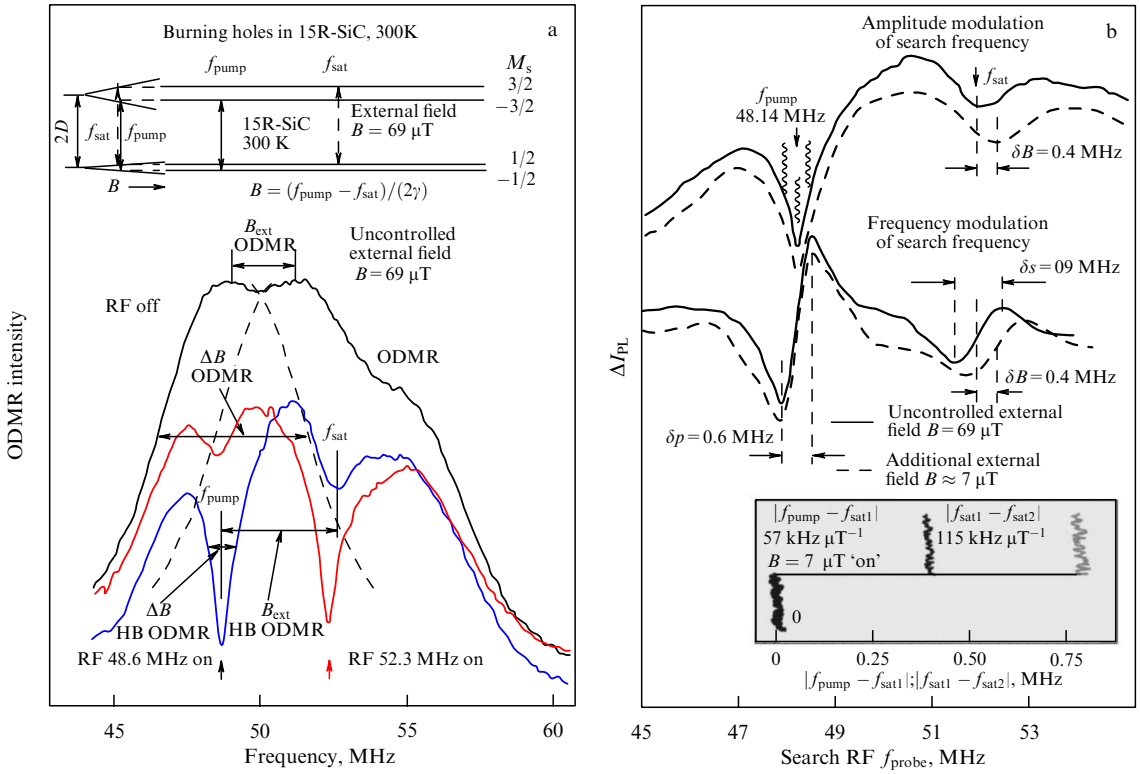

Figure 58. (a) Illustration of HB in a nonuniformly broadened ODMR line in a 15R-SiC crystal at room temperature; the upper part of the figure shows spin-center levels that clarify the HB principle. (b) Results of recording burnt-out dips in a 69 μT field without (solid curves) and with (dashed curves) an additional 7 μT field that correspond to the two modulation schemes indicated in the figure. The inset in the lower part of the figure shows dependences of the differences between frequencies of the dips in the case of stepwise modulation of the external magnetic field.

transition $M_S = +1/2 \leftrightarrow M_S = +3/2$, but with another D. Consequently, it affects the transition ($M_S = -1/2 \leftrightarrow M_S = -3/2$), and another satellite appears at the frequency $f_{s2} = f_p - 2\gamma B$. The coefficient in the linear dependence on the magnetic field is therefore 2γ, twice the coefficient in the case of standard ODMR where the corresponding factor is equal to the gyromagnetic ratio γ. This effect is clearly seen in the magnetic-field splitting of the broad ODMR line, B_{ext}(ODMR), and is approximately twice as large as the difference between the pumping frequency and the satellite frequency B_{ext}(HB ODMR). Both satellites can be used to measure magnetic fields, and the distance between them is $f_{s1} - f_{s2} = 4\gamma B$: the factor in the linear dependence on the magnetic field is doubled again to increase to 4γ.

Thus, to determine the magnetic field, satellite frequencies are measured that depend on splitting Zeeman levels for the ground quadruplet spin state $S = 3/2$ of spin centers in SiC; next, based on the frequency difference, the formula for Zeeman splitting of spin levels is used to calculate the magnetic field to be measured, in which the crystal area excited by focused laser radiation is located.

Figure 58b shows an enlarged image of two detection circuits: the diagram in the upper part corresponds to low-frequency modulation of an RF probing power with a second RF pumping applied, $f_p = 48.14$ MHz, and the diagram in the lower part corresponds to low-frequency modulation of the RF probing power with the RF pumping applied; the satellite frequency f_s that corresponds to a noncompensated external field of 69 μT is also displayed. For both detection schemes spectra are shown that are recorded if an additional external magnetic field of 7 μT is applied (dashed curves); a frequency shift of the satellites is seen. The inset in Fig. 58b shows how the frequency differences $|f_p - f_{s1}|$ and $|f_{s2} - f_{s1}|$, which are used to determine the local magnetic field in the bulk of the crystal excited by a focused laser beam, change when the 7 μT external magnetic field is varied in a stepwise manner; they correspond to the formulas $B = |f_p - f_{s1}|/(2\gamma)$ or $B = |f_{s2} - f_{s1}|/(4\gamma)$ for the magnetic field. Given the noise level, the accuracy of measuring the magnetic fields is of the order of 1 μT Hz$^{-1/2}$.

Cross-relaxation method. Discussed above is the phenomenon of level anti-crossing in the ground state of spin centers, which is used for purely optical measurement of magnetic fields. Fine structure splitting of spin centers in an excited state exhibits strong temperature dependence; we proposed to use this feature to measure temperature using level anti-crossing in an excited state (ES) (ES LAC).

A disadvantage of the proposed method is that the width of the ES LAC, which determines the lifetime in the excited state, is rather large and cannot be reduced. Therefore, we propose to use the physical phenomenon of cross-relaxation of the energy levels of optically active (referred to as 'bright') spin centers with the quadruplet spin state $S = 3/2$ and optically inactive (referred to as 'dark') centers with the triplet state $S = 1$ that exhibit a strong temperature dependence of fine-structure splitting $D(T)$ and are contained in a hexagonal or rhombic SiC crystal.

Figure 59 shows the intensity of PL (ΔPL) of spin centers in a 15R-SiC crystal as a function of the applied magnetic field in the region of spin level anti-crossing in the excited state and in the region of cross-relaxation between the bright centers in the quadruplet spin state and dark centers in the triplet state.

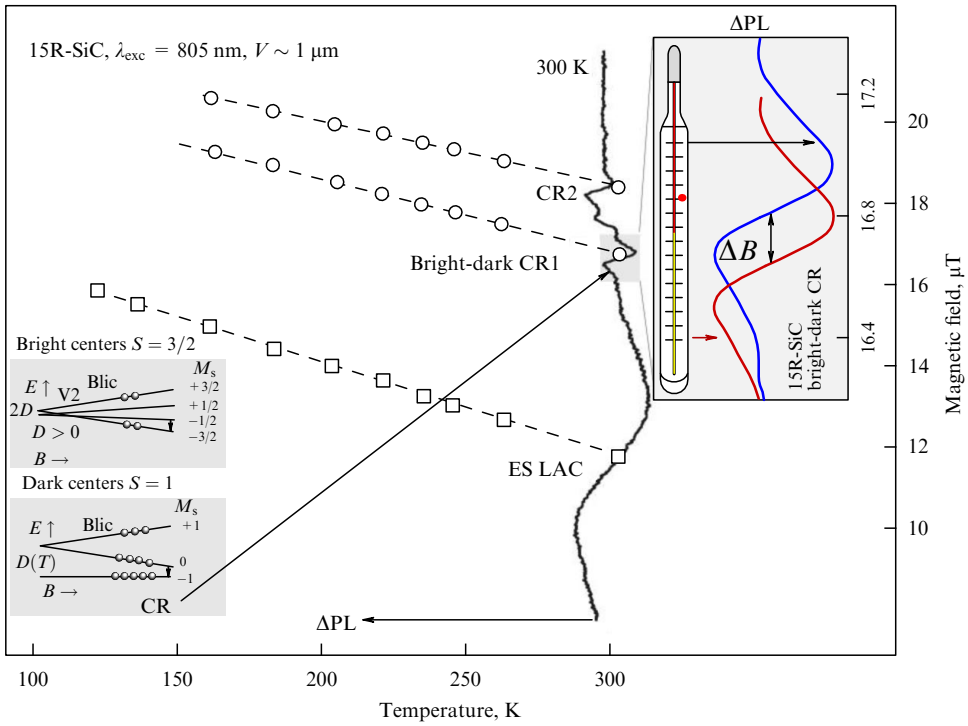

Figure 59. Illustration of temperature measurement based on changes in the PL intensity (ΔPL) of spin centers in a 15R SiC crystal as a function of the magnetic field in the region of anti-crossing of spin levels in an excited state (ES LAC) and in the region of cross-relaxation (CR) between bright centers in quadruplet spin states and dark centers in the triplet spin state. The insets in the left-hand side show the spin levels for the bright ($S = 3/2$) and dark ($S = 1$) centers; arrows conventionally show the direction of the magnetic field for the CR signal. The inset in the right-hand side shows the (enlarged) shift of the CR1 line when temperature varies within the scale of a medical thermometer.

Broken lines shows the dependences of ES LAC and CAR signals on temperature, which can be used as calibrating curves; experimental data are shown as squares (ES LAC) and circles (CR). The insets in the left-hand part of the figure show spin sublevels for the bright ($S = 3/2$) and dark ($S = 1$) centers and the magnetic field at which their CR occurs. The inset in the right-hand part shows on an enlarged scale how the CR1 line shifts if the temperature varies within the limits of the medical thermometer scale.

It can be seen that the CR line is approximately an order of magnitude narrower than the ES LAC line, while the temperature dependence of the positions of these lines is virtually the same.

Spin Hamiltonian (6.1) can be used to calculate energy levels of centers of both types with $S = 3/2$ and $S = 1$, between which CR occurs; the value of γ is virtually the same for these centers. We are only interested in transitions between the bright-center levels that result in changes in the PL intensity. To find the magnetic fields corresponding to CR, the energy differences for the centers with $S = 3/2$ and $S = 1$ should be set equal, yielding the absolute value as a result: $B = |D(T) - 2D|/(2\gamma)$.

The temperature dependence of the magnetic field B_{CR} that corresponds to CR in the range 150–300 K in a 15R-SiC crystal (see Fig. 59) can be approximated with a linear function $B_{CR} = B_0 - kT$, where k is a factor (dimension mT K^{-1}) in the linear dependence of the CR peak on the temperature and T is the temperature measured in kelvin. For the CR1 and CR2 peaks, we have $B_{CR1} = 21.8$ mT – 0.017 mT $K^{-1} \times T$ and $B_{CR2} = 23.8$ mT – 0.018 mT $K^{-1} \times T$.

Scanning device for diagnosing magnetic and temperature fields. Sensors based on SiC micro- or nanocrystals containing an ensemble of highly localized spin color centers, which are placed into an atomic-force microscope probe, can be located in the immediate proximity to external sources of magnetic fields. Studies were conducted using a radio spectroscopic facility that includes a scanning magnetic resonance spectrometer engineered by combining an ASM and a microscope manufactured by NT-MDT Spectrum Instruments. In performing measurements using this facility, an array of spin color centers (down to a single center) is created in a nanosize SiC crystal located on the probe tip, which can be placed close to the magnetic field source or the temperature source at a distance of several nanometers.

Figure 60a shows the element of the scanning microscope based on a micro- or nanocrystal of SiC with spin centers, which is located on the ASM cantilever and performs as a sensitive magnetometer (thermometer) with a submicrometer spatial resolution. Another experimental setup is possible based on a scanning near-field microscope; an SiC nanocrystal can be fixed directly to the end of a bent and cone-shaped optical fiber. The most promising feature is the unique property of PL and excitation of spin-center PL: the wavelength at which the PL of these centers is excited and detected lies in the pass-band of fiber optics and biological objects.

Figure 60b shows how an SiC nanoflake is manipulated and captured at the probe tip: shown sequentially are ASM images of an agglomerate of SiC nanoflakes prior to and in the process of manipulation and a scanning-microscope image of the nanoflake (indicated by a broken-line oval, height 100 nm) captured by the ASM probe cantilever. Figures 60c, d show 6H-SiC nanocrystals with spin centers located on the tip of a standard silicon probe of a scanning ASM and PL of SiC spin centers and (Si) Raman scattering

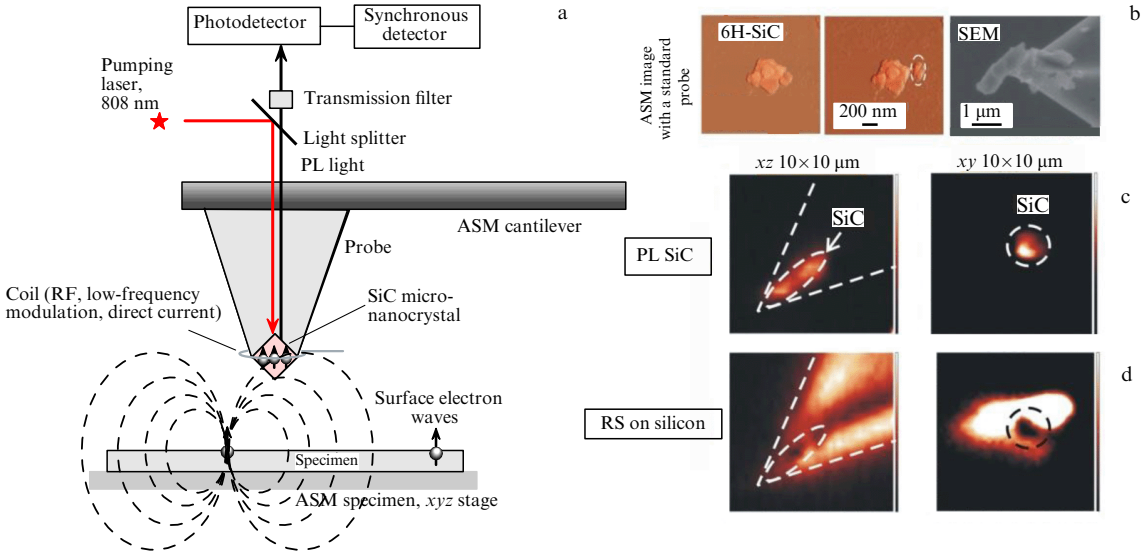

Figure 60. (a) Scanner based on a micro- or nanosize SiC crystal with spin centers placed on an ASM tip that is used as a sensitive magnetometer or thermometer with submicrometer spatial resolution. (b) Manipulations with an SiC nanoflake, capture of this nanoflake on the probe tip, and an SEM image after the capture of the nanoflake on the ASM probe tip. (c, d) 6H-SiC nanocrystals with the spin center located on the tip of a standard silicon ASM probe. (c) PL of spin centers in 6H-SiC nanocrystal and (d) Raman scattering on a silicon probe.

recorded using a standard silicon NSG-10/Pt probe. The PL spectrum of a 6H-SiC nanocrystal is shown in the inset in Fig. 58a.

Next, all the effects listed above can be used to measure magnetic and temperature fields near the ASM probe tip on which SiC micro- and nanocrystals with spin centers are placed. PL can be excited in different ways, depending on the design of the microscope. An important advantage of the method is the possibility of using the same ensemble of spin centers to record magnetic and temperature fields while using various states of the spin centers (such a detection method cannot be realized with NV centers in diamond).

Spin-color centers in SiC can be considered informative microscopic atomic-size probes for local diagnostics of a polytype composition of SiC. The properties of the spin centers of each polytype are unique; moreover, even within the same polytype, the center can be located in various nonequivalent positions in the lattice. Because spin-center parameters (see Table 4) are 'fingerprints' of some polytypes, we used them to control the polytype composition of a single crystal 15R-SiC. Unlike ODMR control, the use of Raman scattering failed to identify the presence of other polytypes. The ODMR method can also be used to identify silicon carbide, also known as carborundum, in nature, including extraterrestrial space, by detecting optically induced radio-frequency emissions of spin color centers (see Fig. 56).

6.2 Graphene on SiC: production, exploration, and possible applications

6.2.1 Growth of graphene foils and studies of their parameters. Graphene is currently regarded as one of the most promising materials that can be used as a foundation of the component base of actively developing nanoelectronics [217]. The use of graphene enables circumventing limitations intrinsic to standard silicon electronics as regards the degree of miniaturization and energy consumption of devices. This advancement is due to the unique physical properties of graphene, of which one of the most important is a very high mobility of charge carriers at room temperature. Various technologies used to produce graphene and thermal physical properties of graphene foils are analyzed in detail in [218].

A promising technology for synthesizing graphene and enabling production of a high-quality material and the possibility of integration into industrial-scale manufacturing is thermal destruction of the surface of semi-insulating silicon-carbide substrate. Thermal destruction can be performed both in a vacuum [219, 220] and in an inert-gas environment [221–224]. The technologies intended for the production of graphene on SiC in a vacuum and argon differ not only by the environment in which growth occurs, but also by the growth temperatures and the orientation of the substrate surface on which graphene is formed. Changes in technological parameters are due to changes in growth kinetics as a result of partial suppression by argon of the sublimation of silicon-carbide components from the substrate surface. Owing to this, it is now possible to use a more thermally stable Si-face of SiC substrate, which in turn resulted in a decreased rate of graphene growth and enabled production of uniform monolayer (ML) graphene foils [225].

Figure 61 shows sets of Raman scattering (RS) spectra of graphene foils grown using the thermal destruction technique of a 4H-SiC polytype in a vacuum (Fig. 61a) and in an argon atmosphere (Fig. 61b). The spectra were measured on a specimen surface of 12.5×12.5 μm^2. Table 5 contains full widths at half maximum (FWHM) of the phonon lines G and 2D that enable an assessment of the structural perfection of two films. Significantly larger $\mathrm{FWHM_G}$ values of the film grown in a vacuum are indicative of its lower structural perfection. This conclusion is also evidenced by the ratio of integral intensities $I_\mathrm{D}/I_\mathrm{G}$, which is used for quantitative assessment of the graphene defectiveness degree [226]. We can see that the distribution maximum of the $I_\mathrm{D}/I_\mathrm{G}$ ratio for the film grown in a vacuum is close to 0.5 (Fig. 61c), which corresponds to the defect density in the crystal lattice $N_\mathrm{d} \sim 5 \times 10^{11}$ cm^{-2} [227]. The same parameter for the film grown in the argon atmosphere is significantly smaller, ~ 0.08

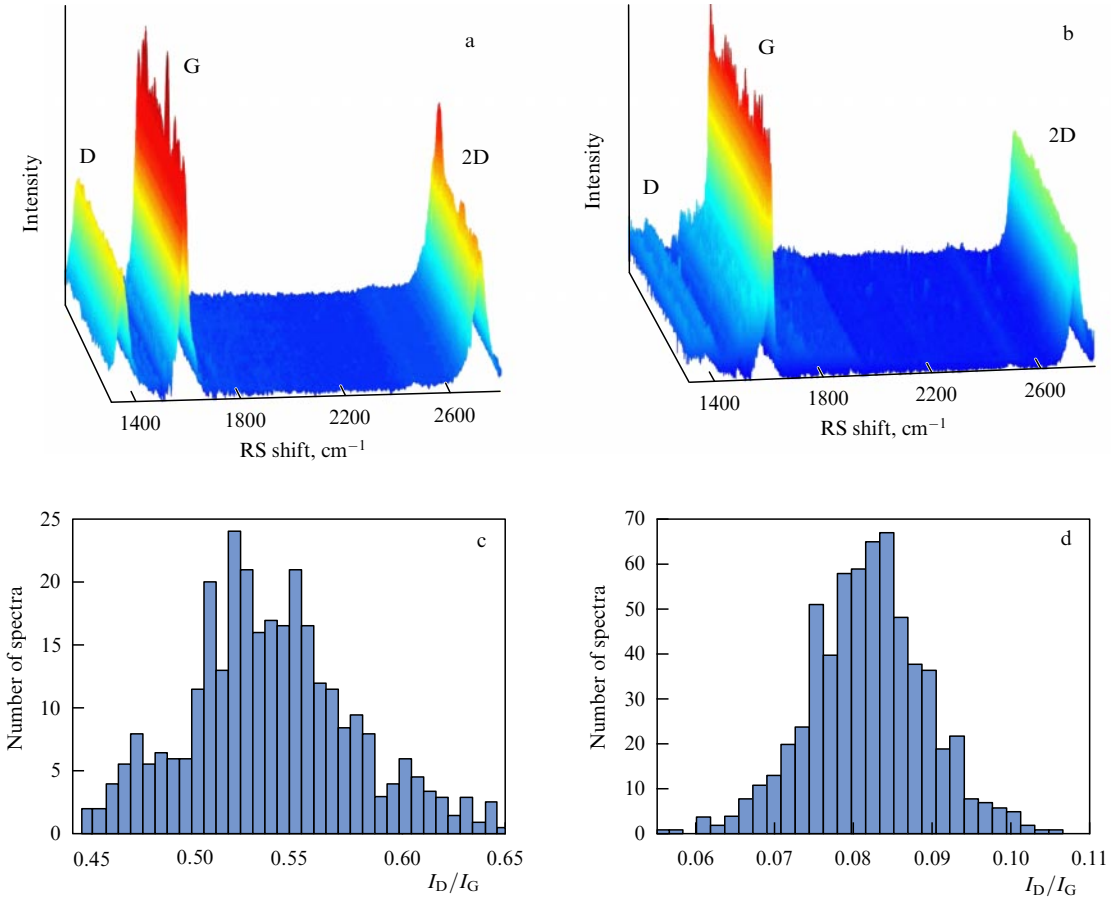

Figure 61. (Color online.) Sets of RS spectra of graphene specimens grown (a) in a vacuum and (b) in an argon atmosphere. SiC substrate spectrum subtracted from the original spectra. Histograms of the I_D/I_G ratio for the graphene grown (c) in a vacuum and (d) in an argon atmosphere.

Table 5. Comparison of structural and transport characteristics of graphene films grown in a vacuum and an argon atmosphere [229].

Growth technology	FWHM$_G$, cm^{-1} (see Fig. 61)	FWHM$_{2D}$, cm^{-1} (see Fig. 61)	I_D/I_G (see Fig. 61)	Film thickness (number of layers)	Conductivity type	μ_{max}, cm^2 V^{-1} s^{-1}	Q, cm^{-2}
In vacuum	30–32	55–60	0.45–0.55	7–9	p-type	$\sim$ 100 (4.2 K)	5×10^{12}
In argon	15–16	33–34	0.07–0.09	1–2	n-type	6000 (300 K)	$7 \times 10^{11} - 1 \times 10^{12}$

(Fig. 61d), implying that the defect density in the crystal lattice is also lower, $N_d < 10^{10}$ cm^{-2}. It was found that the 2D line in most of the spectra for the film grown in the argon atmosphere is symmetrically shaped and well approximated with a single Lorentz contour, a signature of monolayer graphene [228]. The estimated thickness of the graphene foil obtained using the thermal destruction technique in a vacuum on the C-face is 7–9 monolayers [218].

To prepare the obtained graphene films for electrophysical measurements, test structures in the Hall-bar geometry were made on the specimen surface. The topology of the required structures was formed using the technique of standard contact lithography and a specially designed set of mask plates.

The density and mobility of charge carriers in the graphene grown in an argon atmosphere were measured at room temperature using an Accent HL5500PC device in a magnetic field of 0.314 T. The sign of the Hall signal for the structures under study indicates that they are electron-conductivity types. The charge carrier density (Q) in the 2D electron gas of graphene was $7 \times 10^{11} - 3 \times 10^{12}$ cm^{-2}, and the maximum mobility of electrons in the films under study was 6000 cm^2 V^{-1} s^{-1}. For comparison, Table 5 shows the mobility and density of charge carriers for the films grown in a vacuum [219]; according to Hall measurements, they are hole-conductivity types. Although the charge carrier mobility for the vacuum-grown graphene was measured at the liquid helium temperature, the mobility values are more than an order of magnitude smaller than those obtained at room temperature for the films grown in an argon atmosphere.

Figure 62 shows the electron mobility as a function of the 2D density of charge carriers in nonintercalated graphene grown in an argon atmosphere on an Si-face. The curve is plotted using results of the measurements performed by various research groups on graphene specimens grown under various conditions [221–224]. It is clearly seen that electron mobility in graphene increases as the 2D density of charge carriers decreases. The mobility in the films grown with an electron density of less than 10^{12} cm^{-2}, which was found in [219], attains theoretically calculated values for the intrinsic-conductivity graphene at $T = 300$ K without hydrogen intercalation [220].

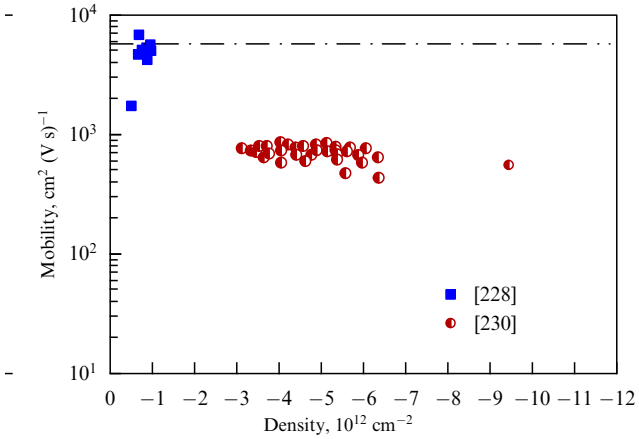

Figure 62. Mobility of charge carriers measured by various research teams in specimens of nonintercalated graphene [229, 231]. The dashed–dotted line shows the theoretical prediction for the limit mobility for graphene specimens of the given type [233].

A conclusion can thus be drawn that the method of thermal destruction of the surface of SiC (0001) in an argon atmosphere under certain conditions of growth (argon pressure of 700–760 Torr, temperature of 1800 – 1850 °C, growth time of 10 min) enables the production of high-quality monolayer graphene films with a high mobility of charge carriers close to that theoretically predicted for the Si-face. This result opens ways to use the developed technology to produce graphene-based devices.

6.2.2 Graphene-based sensors. Graphene, being a 2D material, is known to exhibit a set of unique electrophysical properties:

- high mobility of charge carriers combined with their low density;
- maximum possible surface-to-volume ratio;
- low noise level.

Owing to the combination of these properties, adsorption of a minimal amount of an impurity on the graphene surface can significantly alter its overall conductance. Graphene is therefore a very promising material for manufacturing gas sensors.

It was reported in [230] that graphene can detect the adsorption of even a single molecule. The resistance of a conductor is known to be determined by both the density of charge carriers and their mobility. Adsorbed gas molecules behave, depending on their charge, like donors or acceptors, i.e., they modify the density of mobile charge carriers. Adsorbed substances also create additional scattering centers and change the mobility of carriers. As a result, the resistance of the film decreases or increases, depending on the adsorbed-molecule type.

To purify a graphene detector, passed through it is a current of about 10 mA, an amperage sufficient to heat the structure to the extent that gas particles are desorbed. This purification mechanism does not affect the efficiency of gas detection: gas sorption–desorption is fully reversible, implying that the device can be used many times.

We note that a sensor was made in [230] using exfoliated graphene. Graphene films produced using the exfoliation technology have better structural perfection; however, their dimensions are small and shape is irregular, as a result of which they are not promising for commercial manufacturing.

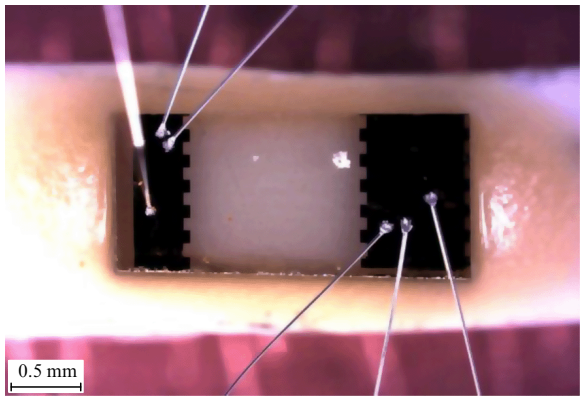

Figure 63. Gas sensor chip. The light area is graphene, and the dark area is metal ohmic contacts with attached wires.

Sensor structure was formed on a graphene film using laser photolithography and an AZ5124 photoresist material [231, 232] (Fig. 63). Excessive graphene was removed from the substrate surface by etching in an oxygen–argon plasma. Ohmic Ti/Au contacts (5/50 nm) were produced by the explosive photolithography method after metal was deposited on the photoresist surface by electron-beam evaporation. The sensor chip was fixed in a holder using two Pt100 resistors. One of the resistors was used to measure temperature, and the other as a heater. Purified air was used as a carrier gas. The sensor sensitivity r, expressed as a percentage, is defined as a relative change in the specimen resistance in the presence of the detected gas in the gas mixture:

$$r = \frac{R - R_0}{R_0},$$

where R is the resistance of the sensor when gas is supplied and R_0 is the initial resistance in the absence of the gas in inflowing air.

Figure 64 shows the relative change in the resistance of a graphene-based sensor in the presence of NO_2 in a gas mixture (time intervals when the gas was introduced are shown with light-grey bars) at a temperature of 20 °C.

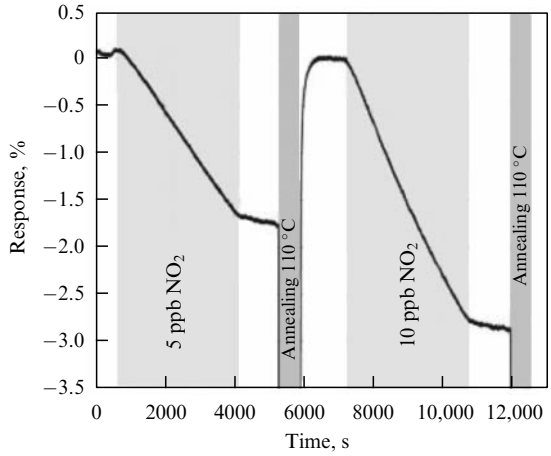

Figure 64. Response of a graphene-based gas sensor as a function of the NO_2 concentration in a gas mixture at 20 °C. The time intervals when the gas is supplied are shown with light grey bars, and annealing periods with dark grey bars.

Because the NO_2 desorption rate at room temperature is very low, to reset the sensor after each exposure session, it was annealed at a temperature of 110 °C [233, 234]. The sensor response amplitude for an NO_2 concentration of 10 ppb (parts per billion) was about 3% for 1-hour-long exposure to the gas mixture. This sensitivity of sensors is quite sufficient for environmental monitoring.

We note that one of the major shortcomings of the graphene gas sensor is that it is not selective. Indeed, it is impossible to determine, based on changes in conductivity, which specific molecule was adsorbed by the graphene surface. Moreover, contributions of some molecules have opposite signs, as a result of which the total change in resistance can be close to zero. The issue of graphene-based sensor selectivity can be resolved by using the antigen–antibody reaction. Components of the pair can interact only with each other and not with any other protein. Antigen markers specific to a single disease or a group of diseases are known to appear in blood at certain stages of many human diseases. These antigens can react with specific antibodies preliminarily deposited on a graphene-sensor surface. Similarly to the gas sensor, the reaction results in changing the graphene-film resistance.

The use of antigen–antibody pairs enables resolving the issue of biosensor selectivity and opens broad prospects for the application of graphene-based sensors in medicine and biology. This approach may result in creating small-size biosensors that can detect diagnostically significant markers of diseases in biological fluids, in an express-analysis mode, including those markers that are currently detected only using a labor- and time-consuming immunoferment analysis [235].

Ti/Au contacts with graphene were formed using electron-beam evaporation and explosive photolithography. A sensor chip 2×2 mm in size was glued to a ceramic holder, and soldered connections were made using Au wires. The conducting channel of the graphene sensor was modified using a denitrating reaction.

To develop a technology for producing graphene-based biosensors, an immunochemical system was chosen that consists of fluorescein and monoclonal antibodies (McABs) binding fluorescein in the form of both free molecules and a chemical group covalently attached to protein carriers. The molecular mass of fluorescein (0.332 kDa) is comparable to the dimensions of a number of biologically significant markers such as hormones, nucleotides, and some short peptides.

Fluorescein has been used for many years as a fluorochrome for labeling the antibodies used in luminescent microscopy. Its isothiocyanate derivative (fluorescein isothiocyanate, FITC) under mild conditions forms stable covalent bonds where the properties of modified proteins change insignificantly, and the number of attached fluorochrome molecules can be determined using the spectrophotometric technique [236]. Similarly to a free molecule, fluorescein covalently attached to proteins absorbs light with a wavelength of 488 nm and emits in the yellow–green (495–522 nm) parts of the spectrum [237].

To develop a technology for depositing antibodies on the surface of graphene, mouse McABs against fluorescein (antibody code F2A3) were used, which were produced in the Hybridoma Technology Laboratory of the Granov Russian Research Center of Radiology and Surgical Technologies. A graphene specimen was placed in a 2 μM solution of 4-nitrobenzene-diazonium-tetrafluoroborate (NDT) and in a 0.1 M solution of tetrafluoroborate tetrabutylammonium in acetonitrile. After nitrophenyl had attached to the graphene surface, the nitrophenyl groups were reduced to phenylamine ones. Electrochemical reaction was performed in a 0.1 M KCl solution in a 9:1 mixture of water and ethyl alcohol. A constant voltage of −0.9 V was applied between the Ag/AgCl electrode and the graphene electrode [238]. Activated graphene specimens were immersed into an F2A3 antibody solution and maintained there for 5 hours at $T = 4$ °C and were afterwards rinsed with water and dried. Sensor response was measured in the mode of constant applied voltage (50 mV); variation of the current flowing through the graphene resistor was recorded. The data response r to the measured reagent was calculated using the formula $r = (I - I_0)/I_0$, where I is the current passing through the sensor and I_0 is the current prior to adding the reagent. Measurements were performed in a borate buffer solution. Testing the graphene-based sensor with the McAB-against-fluorescein deposited on its surface showed that the electric resistance of the sensor noticeably changed when it contacted the solutions that contain a low-molecular ligand with a concentration of 1 or 10 ng ml^{-1} (Fig. 65).

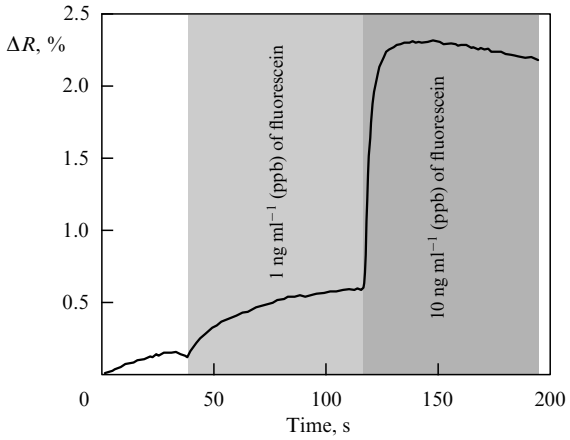

Figure 65. Variation in the resistance (ΔR) of a sensor in contact with solutions containing free fluorescein in the concentrations shown in the plot. The abscissa axis shows the duration of contact with the solutions.

A sample of laboratory-made bovine serum albumin conjugated with fluorescein (F-BSA-5) was used as a high-molecular ligand in [239]. The molecular mass of F-BSA-5 (69 kDa) is comparable to the dimensions of proteins used as markers of human diseases. Each chemical group of fluorescein included in the conjugate with F-BSA-5 contributed about 5% to the molecule mass.

Spectrophotometry data show that the employed conjugate contained three fluorescein groups per F-BSA-5 molecule. Upon contact with a solution of high-molecular ligand (F-BSA-5), changes were detected in the electric resistance of the sensor at the conjugate concentration of 1.37–3.11 ng ml^{-1} (Fig. 66). After having been in contact with the solution that contained the maximum F-BSA-5 concentration, the sensor maintained its capacity to respond to adding a free low-molecular ligand to the solution in a concentration of 1 ng ml^{-1}. The data obtained show that the graphene-based sensor with McAB deposited on its surface can adjoin not only low-molecular ligands, such as fluorescein, but also protein molecules whose mass is at least 20 times larger than the size of low-molecular ligands.

Diagnosing human diseases is currently based to a significant extent on determining the concentrations and the

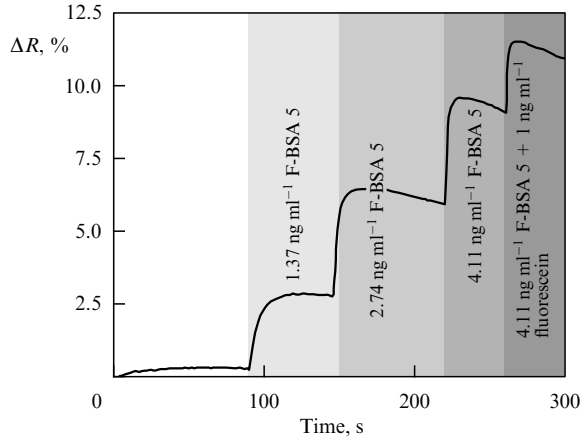

Figure 66. Relative variation of the resistance (ΔR) of a sensor in contact with solutions containing BSA conjugate with fluorescein (F-BSA-5) or a mixture of conjugate and free fluorescein in the concentrations shown in the plot. The abscissa axis shows the duration of contact with the solutions [239].

presence in blood of certain marker molecules that are specific to a single disease or a whole group of diseases. Diagnostically significant macromolecules are identified using the labor- and time-consuming immunoferment analysis. Using biological graphene-based sensors will enable the diagnostics of human diseases to be speeded up and technologically enhanced.

7. Conclusions

We have reviewed work on the development of silicon-carbide-based electronics, a significant part of which was done at the Ioffe Institute. We have briefly discussed electrophysical properties of SiC and other broadband semiconductors from the perspective of engineering devices of various types. The possibility of controlling the growth of silicon carbide of various polytypes has been shown.

Over the last fifteen to twenty years, the Laboratory of Power Semiconductor Devices of the Ioffe Institute has developed high-voltage (over 1 kV) 4H-SiC-based diodes in which potential advantages of silicon carbide with regard to power and pulse electronics have materialized.

Parameters of the developed power JBS diodes are not inferior to those of their foreign counterparts (the closed joint-stock company Gruppa Kremnii-L now manufactures JBS diodes using the post-growth technology developed at the Ioffe Institute that was adapted to industrial conditions).

The developed avalanche diodes can dissipate the maximum possible energy in the avalanche pulse mode; the limit to the dissipated energy is set by local self-heating of the diode base region to a temperature so high that the density of intrinsic carriers in 4H-SiC becomes comparable to the dopant density in the diode base.

The developed 4H-SiC SRDDs enabled the development of generators of high-voltage electric pulses with the pulse leading edge of about 100 ps (there are currently no other similar devices with such characteristics).

Analytic models and numerical simulation with the original Issledovanie software package were used to analyze the main processes occurring in 4H-SiC-based power bipolar devices: thyristors, bipolar transistors, and diodes. Atomic-size color centers in bulk and nanocrystal SiC are shown to be promising systems for spintronics, photonics compatible with the passband of fiber optics and living systems, quantum processing of information, and environmental sensing. A technology for producing graphene foils based on the method of thermal destruction of the surface of SiC single crystals is analyzed. These films are shown to feature high structural perfection, owing to which they can be used for engineering gas sensors and biosensors.

References

1. Acheson E G *Chem. News* **68** 179 (1893)
2. Pensl G, Helbig R, in *Festkörperprobleme 30* (Advances in Solid State Physics, Vol. 30, Ed. V Rössler) (Berlin: Springer, 1990) p. 133
3. Round N J *Electrical World* **30** 309 (1907)
4. Losev O V *Zh. Tekh. Fiz.* **1** 718 (1931)
5. Lely J A *Berichte Deutschen Keramischen Gesellschaft* **32** 229 (1955)
6. Vodakov Yu A et al. *Krist. Tech.* **14** 729 (1979)
7. Tairov Yu M, Tsvetkov V F *J. Cryst. Growth* **43** 209 (1978)
8. Chaussende D et al. *Mater. Sci. Forum* **778–780** 3 (2014)
9. Nishino S, Powell J A, Will N A *Appl. Phys. Lett.* **42** 460 (1983)
10. Kong H S et al. *Appl. Phys. Lett.* **51** 442 (1987)
11. Aristov V Yu *Phys. Usp.* **44** 761 (2001); *Usp. Fiz. Nauk* **171** 801 (2001)
12. Edmond J A, Kong H-S, Carter C H (Jr.) *Physica B* **185** 453 (1993)
13. Palmour J W et al. *Physica B* **185** 461 (1993)
14. Johnson E O *RCA Rev.* **26** 163 (1965)
15. Vavilov V S *Phys. Usp.* **37** 269 (1994); *Usp. Fiz. Nauk* **164** 287 (1994)
16. Lebedev A A, Chelnokov V E *Semiconductors* **33** 999 (1999); *Fiz. Tekh. Poluprovodn.* **33** 1096 (1999)
17. Yong L et al. *J. Semicond.* **34** 054007 (2013)
18. Vavilov V S *Phys. Usp.* **39** 757 (1996); *Usp. Fiz. Nauk* **166** 807 (1996)
19. Leonard R T et al. *Mater. Sci. Forum* **600–603** 7 (2009)
20. Choi J-W et al. *Mater. Sci. Forum* **924** 23 (2018)
21. Jenny J R et al. *Mater. Sci. Forum* **457–460** 35 (2004)
22. Vodakov Yu A, Mokhov E N, USSR invention certificate No. 403275 (1970); Patent USA No. 414572 (1979)
23. Mokhov E N et al. *Mater. Sci. Eng. B* **46** 317 (1997)
24. Vodakov Yu A, Mokhov E N, in *Vacuum Science and Technology. Nitrides as Seen by the Technology* (Eds T Paskova, B Monemar) (Trivandrum: Research Signpost, 2002) p. 59
25. Mokhov E N et al. *J. Cryst. Growth* **281** 93 (2005)
26. Mokhov E N et al. *J. Cryst. Growth* **181** 254 (1997)
27. Karpov S Yu et al. *J. Cryst. Growth* **173** 408 (1997)
28. Segal A S et al. *J. Cryst. Growth* **208** 431 (2000)
29. Simin D et al. *Phys. Rev. X* **6** 031014 (2016)
30. Fuchs F *Sci. Rep.* **3** 1637 (2013)
31. Vodakov Yu A, Lomakina G A, Mokhov E N *Sov. Phys. Solid State* **24** 780 (1982); *Fiz. Tverd. Tela* **24** 1377 (1982)
32. Vodakov Yu A et al., Patent USA No. 6,428, 621 B1, Aug. 6 (2002)
33. Matukov I D et al. *J. Cryst. Growth* **266** 313 (2004)
34. Argunova T S et al. *CrystEngComm* **16** 8917 (2014)
35. Mokhov E N, Nagalyuk S S *Tech. Phys. Lett.* **37** 999 (2011); *Pis'ma Zh. Tekh. Fiz.* **37** (21) 25 (2011)
36. Mokhov E N, Nagaluik S S, Soltamov V A *Mater. Sci. Forum* **897** 7 (2017)
37. Kimoto T, Cooper J A *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications* (Singapore: Wiley, 2014)
38. Ivanov P A, Ignat'ev K I *Mater. Sci. Forum* **264–268** 809 (1998)
39. Ivanov P A, Potapov A S, Samsonova T P *Semiconductors* **43** 185 (2009); *Fiz. Tekh. Poluprovodn.* **43** 197 (2009)
40. Potapov A S, Ivanov P A, Samsonova T P *Semiconductors* **43** 612 (2009); *Fiz. Tekh. Poluprovodn.* **43** 640 (2009)
41. Ivanov P A et al. *Semiconductors* **47** 81 (2013); *Fiz. Tekh. Poluprovodn.* **47** 83 (2013)
42. Grekhov I V et al. *Semiconductors* **42** 211 (2008); *Fiz. Tekh. Poluprovodn.* **42** 211 (2008)
43. Ivanov P A et al. *Semiconductors* **42** 858 (2008); *Fiz. Tekh. Poluprovodn.* **42** 878 (2008)
44. Ivanov P A et al. *Semiconductors* **43** 505 (2009); *Fiz. Tekh. Poluprovodn.* **43** 527 (2009)

45. Ivanov P A et al. *Semiconductors* **44** 653 (2010); *Fiz. Tekh. Poluprovodn.* **44** 680 (2010)
46. Ivanov P A et al. *Semiconductors* **45** 1374 (2011); *Fiz. Tekh. Poluprovodn.* **45** 1427 (2011)
47. Ivanov P A et al. *Semiconductors* **46** 397 (2012); *Fiz. Tekh. Poluprovodn.* **46** 411 (2012)
48. Ivanov P A et al. *Semiconductors* **43** 1209 (2009); *Fiz. Tekh. Poluprovodn.* **43** 1249 (2009)
49. Ivanov P A et al. *Semiconductors* **45** 668 (2011); *Fiz. Tekh. Poluprovodn.* **45** 677 (2011)
50. Sze S M *Physics of Semiconductor Devices* (New York: Wiley, 1981); Translated into Russian: *Fizika Poluprovodnikovykh Priborov* Vol. 1 (Moscow: Mir, 1984)
51. Gerardi G J et al. *Appl. Phys. Lett.* **49** 348 (1986)
52. Ivanov P A, in *2nd European Conf. on Silicon Carbide and Related Materials, September 2–4, 1998, Montpellier, France*. Abstracts, p. 303
53. Ivanov P A et al. *Tech. Phys. Lett.* **23** 798 (1997); *Pis'ma Zh. Tekh. Fiz.* **23** (10) 55 (1997)
54. Waldrop J R et al. *J. Appl. Phys.* **72** 4757 (1992)
55. Andreev A N et al. *Semiconductors* **29** 957 (1995); *Fiz. Tekh. Poluprovodn.* **29** 1828 (1995)
56. Afanas'ev A V et al. *Tech. Phys.* **46** 584 (2001); *Zh. Tekh. Fiz.* **71** (5) 78 (2001)
57. Ferrero S et al. *Mater. Sci. Forum* **483–485** 733 (2005)
58. Anantharam V, Bhat K N *IEEE Trans. Electron Dev.* **27** 939 (1980)
59. Baliga B J, Ghandhi S K *Solid-State Electron.* **19** 739 (1976)
60. Suh K-D et al. *Solid-State Electron.* **33** 1125 (1990)
61. Wahab Q et al. *Appl. Phys. Lett.* **76** 2725 (2000)
62. Hull B et al. *Mater. Sci. Forum* **600–603** 931 (2009)
63. Ivanov P A et al. *Semiconductors* **51** 374 (2017); *Fiz. Tekh. Poluprovodn.* **51** 390 (2017)
64. Ivanov P A, Samsonova T P, Potapov A S *Semiconductors* **52** 1630 (2018); *Fiz. Tekh. Poluprovodn.* **52** 1527 (2018)
65. Ivanov P A et al. *Radiotekh. Elektron.* (2019), in print
66. Ivanov P A et al. *Semiconductors* **52** 1307 (2018); *Fiz. Tekh. Poluprovodn.* **52** 1187 (2018)
67. Kozlovskii V V *Modifitsirovanie Poluprovodnikov Puchkami Protonov* (Modifying Semiconductors with Proton Beams) (St. Petersburg: Nauka, 2003)
68. RENESAS, AN1968, Nov 9, 2015, https://www.intersil.com/content/dam/Intersil/documents/an19/an1968.pdf
69. Grekhov I V, Mesyats G A *Phys. Usp.* **48** 703 (2005); *Usp. Fiz. Nauk* **175** 735 (2005)
70. Grekhov I V et al. *Solid-State Electron.* **47** 1769 (2003)
71. Grekhov I V et al. *Semiconductors* **37** 1123 (2003); *Fiz. Tekh. Poluprovodn.* **37** 1148 (2003)
72. Ivanov P A, Grekhov I V *Semiconductors* **46** 528 (2012); *Fiz. Tekh. Poluprovodn.* **46** 544 (2012)
73. Ivanov P A, Grekhov I V *Tech. Phys.* **60** 897 (2015); *Zh. Tekh. Fiz.* **85** (6) 111 (2015)
74. Ivanov P A, Grekhov I V *Tech. Phys.* **61** 240 (2016); *Zh. Tekh. Fiz.* **86** (2) 85 (2016)
75. Ivanov P A, Grekhov I V *Tech. Phys.* **63** 86 (2018); *Zh. Tekh. Fiz.* **88** (1) 89 (2018)
76. Ivanov P A et al. *Semiconductors* **50** 883 (2016); *Fiz. Tekh. Poluprovodn.* **50** 900 (2016)
77. Ivanov P A et al. *Solid-State Electron.* **123** 15 (2016)
78. Hjelm M et al. *J. Appl. Phys.* **93** 1099 (2003)
79. Bellotti E et al. *Int. J. High Speed Electron. Syst.* **11** 525 (2001)
80. Ivanov P A et al. *Semiconductors* **49** 1511 (2015); *Fiz. Tekh. Poluprovodn.* **49** 1558 (2015)
81. Ivanov P A et al. *Tech. Phys. Lett.* **44** 229 (2018); *Pis'ma Zh. Tekh. Fiz.* **44** (6) 11 (2018)
82. Dmitriev V A et al. *Electron. Lett.* **24** 1031 (1988)
83. Baier R et al. *Phys. Lett. B* **345** 277 (1995)
84. Levinshtein M E et al., in *SiC Materials and Devices* Vol. 1 (Eds M Shur, S Rumyantsev, M Levinshtein) (Singapore: World Scientific, 2006)
85. Rumyantsev S L et al. *Semicond. Sci. Technol.* **28** 125017 (2013)
86. Rumyantsev S L et al. *Mater. Sci. Forum* **821–823** 893 (2015)
87. O'Brien H et al. *Mater. Sci. Forum* **717–720** 1155 (2012)
88. Dyakonova N V et al. *Electron. Lett.* **33** 914 (1997)
89. Levinshtein M E et al. *IEEE Trans. Electron Dev.* **45** 307 (1998)
90. Levinshtein M E et al. *Semicond. Sci. Technol.* **14** 207 (1999)
91. Ivanov P A et al. *Solid-State Electron.* **44** 2155 (2000)
92. Levinshtein M E et al. *Solid-State Electron.* **47** 699 (2003)
93. Rezaei M A et al. *Mater. Sci. Forum* **778–780** 1021 (2014)
94. Dyakonova N V et al. *Semicond. Sci. Technol.* **13** 241 (1998)
95. Cao L, Li B, Zhao J H *Solid-State Electron.* **44** 347 (2000)
96. Bergman G D *Solid-State Electron.* **8** 757 (1965)
97. Levinshtein M E et al. *Solid-State Electron.* **45** 453 (2001)
98. Mnatsakanov T T et al. *Solid-State Electron.* **46** 525 (2002)
99. Mnatsakanov T T, Rostovtsev I L, Philatov N I *Solid-State Electron.* **30** 579 (1987)
100. Levinshtein M E et al. *IEEE Trans. Electron Dev.* **48** 1703 (2001)
101. Mnatsakanov T T et al. *Solid-State Electron.* **46** 525 (2002)
102. Mnatsakanov T T et al. *Solid-State Electron.* **47** 1581 (2003)
103. Mnatsakanov T T, Yurkov S N, Tandoev A G *Semiconductors* **39** 354 (2005); *Fiz. Tekh. Poluprovodn.* **39** 372 (2005)
104. Yurkov S N et al. *Semicond. Sci. Technol.* **29** 125012 (2014)
105. Xie K et al. *IEEE Electron Dev. Lett.* **17** 142 (1996)
106. Agarwal A K et al. *IEEE Electron Dev. Lett.* **18** 518 (1997)
107. Li B, Cao L, Zhao J H *IEEE Electron Dev. Lett.* **20** 219 (1999)
108. Agarwal A K et al. *Semicond. Sci. Technol.* **16** 260 (2001)
109. Ivanov P A et al. *Electron. Lett.* **35** 1382 (1999)
110. Levinshtein M E et al. *Solid-State Electron.* **46** 1953 (2002)
111. Weiser K et al. *Trans. AIME* **230** 271 (1964)
112. Uvarov A I, in *Physics of p–n Junctions and Semiconductor Devices* (Eds S M Ryvkin, Yu V Shmartsev) (New York: Consultants Bureau, 1971) p. 170
113. Uvarov A I, in *Physics of p–n Junctions and Semiconductor Devices* (Eds S M Ryvkin, Yu V Shmartsev) (New York: Consultants Bureau, 1971) p. 216
114. Suzuki M et al. *IEEE Trans. Electron Dev.* **29** 1222 (1982)
115. Dodson H, Longini R L *IEEE Trans. Electron. Dev.* **13** 478 (1966)
116. Vainshtein S N, Zhilyaev Yu V, Levinshtein M E *Fiz. Tekh. Poluprovodn.* **21** 129 (1987)
117. Gentry F E et al. *Semiconductor Controlled Rectifiers. Principles and Applications of p–n–p–n Devices* (Englewood Cliffs, NJ: Prentice-Hall, 1964)
118. Blicher A *Thyristor Physics* (New York: Springer-Verlag, 1976)
119. Gerlach W *Thyristoren* (Heidelberg: Springer-Verlag, 1981)
120. Korobov V, Mitin V *J. Appl. Phys.* **79** 1143 (1996)
121. Elasser A, Chow T P *Proc. IEEE* **90** 969 (2002)
122. Yurkov S N et al. *Solid-State Electron.* **49** 2011 (2005)
123. Levinshtein M E et al. *Semicond. Sci. Technol.* **20** 793 (2005)
124. Kuz'min V A (Ed.) *Raschet Silovykh Poluprovodnikovykh Priborov* (Calculation of Power Semiconductor Devices) (Moscow: Energiya, 1980)
125. Auston D H *Appl. Phys. Lett.* **26** 101 (1975)
126. Hur J H et al. *IEEE Trans. Electron Dev.* **37** 2520 (1990)
127. Korobov V, Mitin V *J. Appl. Phys.* **79** 1143 (1996)
128. Levinshtein M E et al. *Electron. Lett.* **38** 592 (2002)
129. Dheilly N et al. *Electron. Lett.* **47** 459 (2011)
130. Rumyantsev S L et al. *Semicond. Sci. Technol.* **27** 015012 (2012)
131. Levinshtein M E et al. *Semiconductors* **46** 1201 (2012); *Fiz. Tekh. Poluprovodn.* **46** 1224 (2012)
132. D'yakonov M I, Levinshtein M E et al. *Sov. Phys. Semicond.* **12** 426 (1978); *Fiz. Tekh. Poluprovodn.* **12** 729 (1978)
133. D'yakonov M I, Levinshtein M E et al. *Sov. Phys. Semicond.* **12** 992 (1978); *Fiz. Tekh. Poluprovodn.* **12** 1674 (1978)
134. Yuferev V S, Levinshtein M E, Palmour J W *Semicond. Sci. Technol.* **27** 035004 (2012)
135. Yuferev V S, Levinshtein M E, Palmour J W *Semiconductors* **47** 116 (2013); *Fiz. Tekh. Poluprovodn.* **47** 118 (2013)
136. Yuferev V S, Levinshtein M E, Palmour J W *Semicond. Sci. Technol.* **28** 105009 (2013)
137. Levinshtein M E et al. *Semiconductors* **50** 404 (2016); *Fiz. Tekh. Poluprovodn.* **50** 408 (2016)
138. Rumyantsev S L et al. *Semicond. Sci. Technol.* **29** 115003 (2014)
139. Mnatsakanov T T et al. *Semicond. Sci. Technol.* **29** 055005 (2014)
140. Luo Y, Fursin L, Zhao J H *Electron. Lett.* **36** 1496 (2000)

141. Tang Y, Fedison J B, Chow T P *IEEE Electron Dev. Lett.* **22** 119 (2001)
142. Ryu S et al. *IEEE Electron Dev. Lett.* **22** 124 (2001)
143. Zhang J et al. *Electron. Lett.* **40** 1381 (2004)
144. Miyake H, Kimoto T, Suda J *IEEE Electron Dev. Lett.* **32** 841 (2011)
145. Zhang J et al. *IEEE Electron Dev. Lett.* **27** 368 (2006)
146. Ivanov P A et al. *Solid-State Electron.* **46** 567 (2002)
147. Ivanov P A et al. *IEEE Trans. Electron Dev.* **53** 1245 (2006)
148. Ivanov P A et al. *Semiconductors* **39** 861 (2005); *Fiz. Tekh. Poluprovodn.* **39** 897 (2005)
149. Balachandran S et al. *IEEE Electron Dev. Lett.* **26** 470 (2005)
150. Ghandi R et al. *Mater. Sci. Forum* **679–680** 706 (2011)
151. Gao Y, PhD Thesis (2007); https://repository.lib.ncsu.edu/handle/1840.16/4818 (2008)
152. Buono B et al. *IEEE Trans. Electron Dev.* **58** 2081 (2011)
153. Yuferev V S et al. *Solid-State Electron.* **123** 130 (2016)
154. Vainshtein S N, Yuferev V S, Kostamovaara J T *IEEE Trans. Electron Dev.* **49** 142 (2002)
155. Vainshtein S et al. *Phys. Rev. Lett.* **99** 176601 (2007)
156. Vainshtein S et al. *Appl. Phys. Lett.* **100** 073505 (2012)
157. Dmitriev A P et al. *J. Appl. Phys.* **123** 134503 (2018)
158. Gert A V et al. *Appl. Phys. Lett.* **111** 203503 (2017)
159. Levinshtein M E et al. *Solid-State Electron.* **48** 491 (2004)
160. Ivanov P A et al. *Semicond. Sci. Technol.* **25** 045030 (2010)
161. Stepanenko I P *Osnovy Teorii Tranzistorov i Tranzistornykh Skhem* (Theory of Transistors and Transistor Circuits: a Primer) (Moscow–Leningrad: Gosenergoizdat, 1963)
162. Yuferev V S et al. *Semiconductors* **51** 1194 (2017); *Fiz. Tekh. Poluprovodn.* **51** 1243 (2017)
163. Kordina O et al. *Appl. Phys. Lett.* **67** 1561 (1995)
164. Sugawara Y et al., in *Proc. of Intern. Symp. on Power Semiconductor Devices and Ics, Osaka, Japan* (2001) p. 27
165. Mnatsakanov T T et al. *Semicond. Sci. Technol.* **20** 62 (2005)
166. Mnatsakanov T T et al. *J. Appl. Phys.* **99** 074503 (2006)
167. Mnatsakanov T T et al. *Semiconductors* **41** 1381 (2007); *Fiz. Tekh. Poluprovodn.* **41** 1401 (2007)
168. Ivanov P A et al. *Solid-State Electron.* **50** 1368 (2006)
169. Miyazawa T et al. *J. Appl. Phys.* **118** 085702 (2015)
170. Lax B, Neustadter T *J. Appl. Phys.* **25** 1148 (1954)
171. Gossick B R *J. Appl. Phys.* **27** 905 (1956)
172. Levinshtein M E et al. *Electron. Lett.* **39** 689 (2003)
173. Levinshtein M E et al. *Solid-State Electron.* **48** 807 (2004)
174. Levinshtein M E et al. *Electron. Lett.* **36** 1241 (2000)
175. Levinshtein M E et al. *Solid-State Electron.* **52** 1802 (2008)
176. Levinshtein M E et al. *Semicond. Sci. Technol.* **23** 085011 (2008)
177. Dannhäuser F *Solid-State Electron.* **15** 1371 (1972)
178. Höpfel R A et al. *Phys. Rev. Lett.* **56** 2736 (1986)
179. Mnatsakanov T T et al. *J. Appl. Phys.* **93** 1095 (2003)
180. Mnatsakanov T T, Rostovtsev I L, Filatov N I *Sov. Phys. Semicond.* **18** 807 (1984); *Fiz. Tekh. Poluprovodn.* **18** 1293 (1984)
181. Levinshtein M E, Mnatsakanov T T *IEEE Trans. Electron Dev.* **49** 702 (2002)
182. Levinshtein M E et al. *Semicond. Sci. Technol.* **26** 055024 (2011)
183. Herlet A *Solid-State Electron.* **11** 717 (1968)
184. Jenny J R et al. *J. Appl. Phys.* **100** 113710 (2006)
185. Kuz'min V A et al. *Radiotekh. Elektron.* **33** 609 (1989)
186. Mnatsakanov T T et al. *Semicond. Sci. Technol.* **24** 125010 (2009)
187. Levinshtein M E et al. *Solid-State Electron.* **51** 955 (2007)
188. Gruber A et al. *Science* **276** 2012 (1997)
189. Jelezko F, Wrachtrup J *Phys. Status Solidi A* **203** 3207 (2006)
190. Baranov P G et al. *JETP Lett.* **82** 441 (2005); *Pis'ma Zh. Eksp. Teor. Fiz.* **82** 494 (2005)
191. Baranov P G et al. *JETP Lett.* **86** 202 (2007); *Pis'ma Zh. Eksp. Teor. Fiz.* **86** 231 (2007)
192. Weber J R et al. *Proc. Natl. Acad. Sci. USA* **107** 8513 (2010)
193. Baranov P G et al. *Phys. Rev. B* **83** 125203 (2011)
194. Riedel D et al. *Phys. Rev. Lett.* **109** 226402 (2012)
195. Kraus H et al. *Sci. Rep.* **4** 5303 (2014)
196. Kraus H et al. *Nature Phys.* **10** 157 (2014)
197. Simin D et al. *Phys. Rev. X* **6** 031014 (2016)
198. Widmann M et al. *Nature Mater.* **14** 164 (2015)
199. Christle D J et al. *Nature Mater.* **14** 160 (2015)
200. Anisimov A N et al. *Sci. Rep.* **6** 33301 (2016)
201. Soltamov V A et al. *Phys. Rev. Lett.* **115** 247602 (2015)
202. Anisimov A N et al. *Appl. Magn. Reson.* **49** 85 (2018)
203. Baranov P G et al. *Magnetic Resonance of Semiconductors and Their Nanostructures. Basic and Advanced Applications* (Springer Series in Materials Science, Vol. 253) (New York: Springer, 2017)
204. von Bardeleben H J et al. *Phys. Rev. B* **94** 121202(R) (2016)
205. Carter S G et al. *Phys. Rev. B* **92** 161202(R) (2015)
206. Baranov P G et al., Patent RF No. 2523744 (2014)
207. Anisimov A N et al., Patent RF No. 2617293 (2017)
208. Anisimov A N et al., Patent RF No. 2617194 (2017)
209. Babunts R A et al., Patent RF No. 2607840 (2017)
210. Babunts R A et al., Patent RF No. 2601734 (2016)
211. Anisimov A N et al. *Tech. Phys. Lett.* **43** 355 (2017); *Pis'ma Zh. Tekh. Fiz.* **43** (7) 70 (2017)
212. Anisimov A N et al. *Tech. Phys. Lett.* **42** 618 (2016); *Pis'ma Zh. Tekh. Fiz.* **42** (12) 22 (2016)
213. Soltamov V A, Baranov P G *Phys. Usp.* **59** 605 (2016); *Usp. Fiz. Nauk* **186** 678 (2016)
214. Anisimov A N et al. *JETP Lett.* **104** 82 (2016); *Pis'ma Zh. Eksp. Teor. Fiz.* **104** 82 (2016)
215. Soltamov V A *Phys. Solid State* **57** 891 (2015); *Fiz. Tverd. Tela* **57** 877 (2015)
216. Simin D et al. *Phys. Rev. Appl.* **4** 014009 (2015)
217. Novoselov K S et al. *Nature* **490** 192 (2012)
218. Eletskii A V et al. *Phys. Usp.* **54** 227 (2011); *Usp. Fiz. Nauk* **181** 233 (2011)
219. Lebedev A A et al. *Semiconductors* **45** 623 (2011); *Fiz. Tekh. Poluprovodn.* **45** 634 (2011)
220. Geng Z et al. *Ann. Physik* **529** 1700033 (2017)
221. Robinson J A et al. *Nano Lett.* **11** 3875 (2011)
222. Emtsev K V et al. *Nature Mater.* **8** 203 (2009)
223. Kruskopf M et al. *2D Mater.* **3** 041002 (2016)
224. Händel B et al. *Appl. Surf. Sci.* **291** 87 (2014)
225. Davydov V Yu et al. *Semiconductors* **51** 1072 (2017); *Fiz. Tekh. Poluprovodn.* **51** 1116 (2017)
226. Cançado L G et al. *Nano Lett.* **11** 3190 (2011)
227. Ganesan K et al. *Phys. Chem. Chem. Phys.* **18** 22160 (2016)
228. Ferrari A C, Basko D M *Nature Nanotechnol.* **8** 235 (2013)
229. Lebedev S P et al. *Tech. Phys. Lett.* **43** 849 (2017); *Pis'ma Zh. Tekh. Fiz.* **43** (18) 64 (2017)
230. Schedin F et al. *Nature Mater.* **6** 652 (2007)
231. Usikov A et al. *Key Eng. Mater.* **799** 197 (2019)
232. Novikov S et al. *IEEE Trans. Instrum. Measur.* **62** 1859 (2013)
233. Tedesco J L et al. *Appl. Phys. Lett.* **95** 122102 (2009)
234. Novikov S et al. *Sensors Actuators B* **236** 1054 (2016)
235. Egorov A M, Osipov A P, Dzantiev B B *Teoriya i Praktika Immunofermentnogo Analiza* (Theory and Practice of Immunoferment Analysis) (Moscow: Vysshaya Shkola, 1991) p. 288
236. Jorbágy A, Király K *Biochem. Biophys. Acta BBA Gen. Subjects* **124** 166 (1966)
237. Tengerdy R P, Chang C-A *Analyt. Biochem.* **16** 377 (1966)
238. Tehrani Z et al. *2D Mater.* **1** 025004 (2014)
239. Lebedev A A et al. *Tech. Phys. Lett.* **42** 729 (2016); *Pis'ma Zh. Tekh. Fiz.* **42** (14) 28 (2016)