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GaAs epitaxy on Si substrates: modern status of research and engineering

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Contents

Abstract. **While silicon and gallium arsenide are dominant materials in modern micro- and nanoelectronics, devices fabricated from them still use Si and GaAs substrates only separately. Integrating these materials on the (highest efficiency) substrate of Si has been the subject of much research effort for more than twenty years. This review systematizes and generalizes the current understanding of the fundamental physical mechanisms governing the epitaxial growth of GaAs and its related III–V compounds on Si substrates. Basic techniques available for improving the quality of such heterostructures are described, and recent advances in fabricating device-quality $A^{III}B^{V}$/Si heterostructures and devices on their bases are also presented.**

1. Introduction

Silicon is the basic material of electronics. About 95% of all semiconductor devices are manufactured using silicon substrates. As a carrier, the Si substrate is undoubtedly advantageous due to its small mass, good thermal conductivity, low cost, maximum wafer diameter, and wide prevalence. On the other hand, the electronic engineering materials that come after silicon — III–V compounds, primarily gallium arsenide — are the basic materials of optoelectronics and due to considerably higher carrier mobility form the basis for high-speed special-purpose devices. It has therefore been a natural desire on the part of researchers to bring these materials together on a single — silicon — substrate.

The first step toward this goal is to obtain high-quality thin GaAs layers on an Si substrate, creating so-called artificial, or alternative, substrates. Alternative GaAs-on-Si substrates will have a high market potential as a replacement for the expensive substrates currently used to produce traditional GaAs-based devices, such as microwave devices, solar cells, and photodetectors. Moreover, they enable the development of monolithic integration technology for GaAs elements and silicon integrated circuits (ICs). Using GaAs-on-Si substrates can change the entire production economics related to ICs and the components of GaAs-based optoelectronic devices. The new technology can also revolutionize the technology of manufacturing monolithic ICs based on the combination of gallium arsenide and silicon integrated circuits. A further factor increasingly adding to the interest in GaAs-on-Si technology is silicon IC miniaturization, a trend which in fact pushes these devices to their fundamental size limit. It is becoming possible to increase the speed of ICs without decreasing the size of their constituent elements by using the optical fiber integration of GaAs lasers and photodiodes with silicon-based signal processing circuitry. Of no less importance for present-day semiconductor materials science is the development of high- efficiency cascade solar cells using semiconducting III–V compounds on cheap high-strength silicon substrates.

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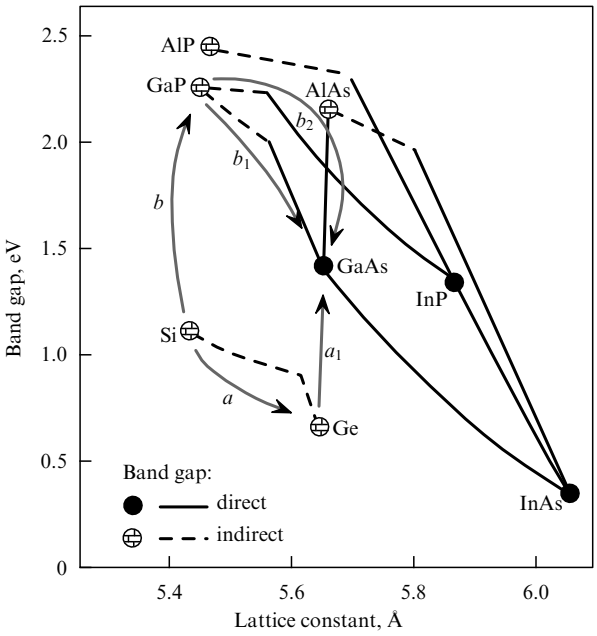

Figure 1. Band gap versus lattice constant for Ge, Si, and III – V compounds. Arrows indicate crystallographic transition pathways from Si to GaAs and III – V compounds based on it.

GaAs crystal can be grown by molecular beam epitaxy (MBE) directly on an Si substrate (see, for example, Refs [1, 2]). However, in this case all the crystal imperfections due to the large mismatch between GaAs and Si in their lattice constants ($\sim 4\%$) and thermal expansion coefficients will be concentrated within the GaAs layer. In recent years, researchers have been placing various kinds of buffer layers between the Si substrate and the GaAs film. In Fig. 1, shown against the background of the lattice constant dependences of the band gaps of the group IV semiconductor materials (Si and Ge) and III – V compounds are the crystallographic transition pathways from silicon to gallium arsenide, on the latter of which AlGaAs/GaAs or InGaAsP/GaAs type heterosystems can be grown by known techniques, and then various devices can be created on their bases. As of today, the pathway explored most is that through germanium (arrows a and a_1 in Fig. 1). The main obstacle here is that the 4% lattice mismatch between Si and Ge produces a large density (up to $10^9 - 10^{10}$ cm^{-2}) of dislocations in the epitaxial Ge. Another pathway — GaAs on Ge (arrow a_1) — poses no problems and has long been successfully probed: Ge is used as a substrate in manufacturing high-efficiency solar cells based on III – V compounds for space applications (see, for example, Refs [3, 4]). A further pathway shown in Fig. 1 by arrows b, b_1, and b_2 passes through GaP whose lattice constant differs from that of Si by 0.37%. Further on, variable-composition buffer layers can be made using the compound GaAsP (arrow b_1) or InGaP (arrow b_2). In this case, the lattice constant transition to GaAs is largely made based on three-component III – V compounds. Thus, the preparation of an artificial GaAs/Si substrate invariably involves a lattice constant change from the Si substrate to the GaAs film, posing a significant obstacle to the development of perfect heterostructures (dubbed 'platforms' in the recent literature).

Another obstacle is the considerable difference in the thermal expansion coefficients between silicon and the III – V compounds. Finally, during the growth of a binary compound like GaAs on a monoatomic semiconductor (Si, Ge), antiphase domain boundaries, which are structural defects specific to such heteroepitaxy, are initiated and penetrate into the film. Whereas the last of these problems is being fairly successfully solved by means of double-layer step formation using misoriented Si substrates and their preepitaxial heat treatment, the first two still remain high on the list of problems yet to be solved in this area of semiconductor materials science. Many research groups have been working for over two decades in this area, but it is only recently that considerable progress has been made in solving the problems listed above.

This review summarizes and systematizes the current understanding of the fundamental physical mechanisms that control the epitaxial formation of III – V compounds on Si substrates and presents the basic technologies for improving the structural characteristics of such heterostructures (HSs). Recent achievements in manufacturing device-quality HSs and their associated instruments are also described.

2. GaAs/Si manufacturing problems. Comparison in terms of general structural perfection

The first successful experiments on growing GaAs on Si substrates date back to the 1980s (see, for example, Refs [1, 2, 5 – 7]). Historically, the way these experiments were conducted was by growing this material directly on Si [1, 2, 8 – 15]. By the last decade of the twentieth century all the basic problems involved were identified and comprehensively reviewed (see Fang et al. [16]). First and foremost is the growth of a polar semiconductor on a nonpolar substrate, an effect which leads to the formation of high-density antiphase domains. It was theoretically predicted and then confirmed by tunneling microscopy (see, for example, Refs [17, 18]) that the clean (001) surface of silicon basically consists of monoatomic steps which have their Si atoms arranged in the form of dimers in such a way that the dimers on one terrace are perpendicular to those of the neighbouring one (Fig. 2a, *1*). Passivating such a surface with arsenic, i.e., coating an Si surface with a monolayer of As — the necessary initial stage for the growth of a polar compound on a nonpolar substrate — leads to the formation of As dimers in such a way that dimers on one terrace are also perpendicular to those on the other.

Let us consider next the atomic structure of a III – V type compound (GaAs being an example). It is known that an As-enriched surface GaAs(001) is terminated by $[1\bar{1}0]$-elongated arsenic dimers. This model, first proposed by Chadi [19], is shown in one of its versions in Fig. 2b. The structure of this surface reproduces itself as the epitaxial growth proceeds. If neighboring Si terraces consist of As dimers directed perpendicular to each other as shown at the bottom of Fig. 2c, then the GaAs nuclei that form on the neighboring terraces will be mutually rotated by 90° around the vertical axis. As seen in Fig. 2c, which displays singularly faceted GaAs crystallites, as the crystallites grow and coalesce, the contacting planes are {111} planes which terminate in atoms of the same species — either As or Ga — resulting in the formation of crystal structure defects known as antiphase defects.

This problem was successfully resolved by using Si substrates deflected through 4° – 6° from the singular (001) plane (see, for example, Ref. [9]). It was shown by Olsha-

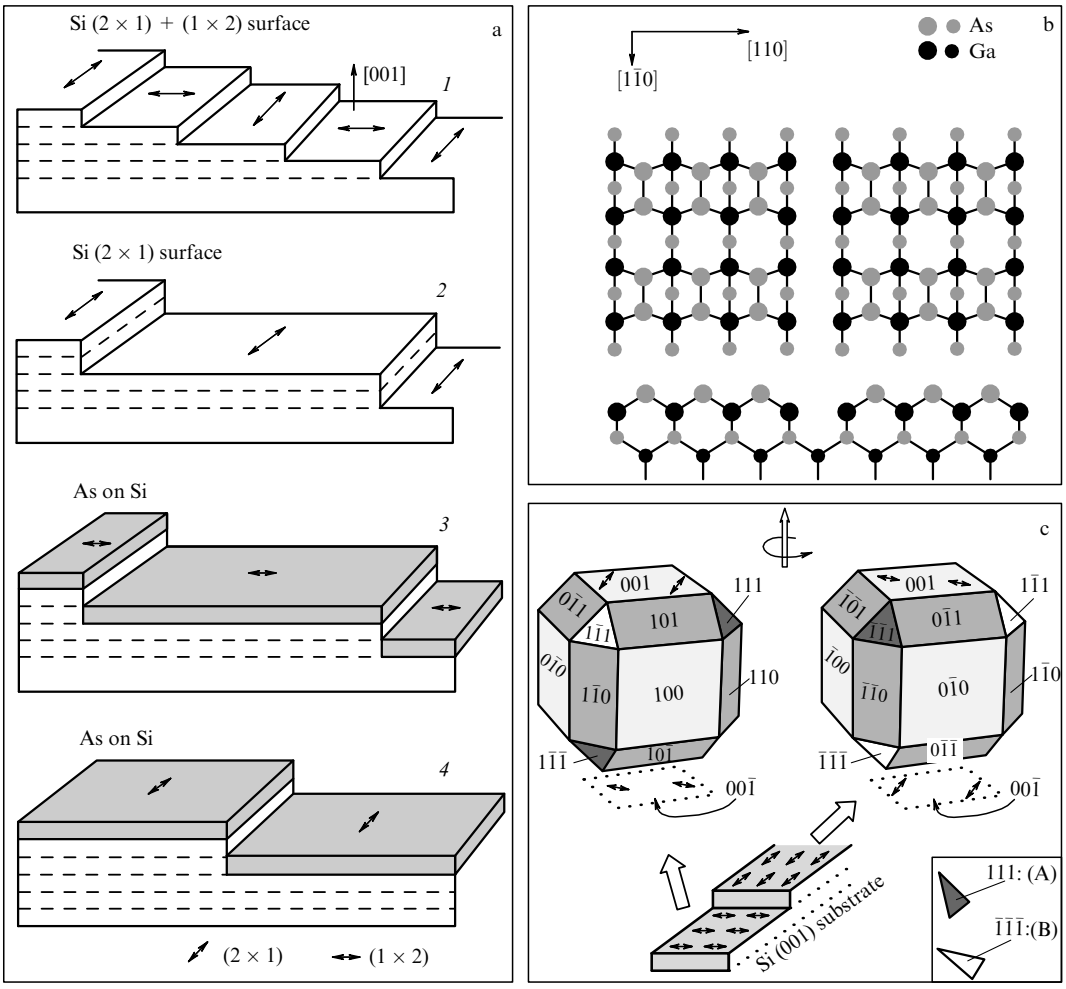

Figure 2. (a) A schematic of the step structure of a vicinal surface having its normal deflected by a few degrees from [001] to [110] (taken from Ref. [21]). (b) Schematic representation of a GaAs(001) (2 × 4) surface reconstructed with a three-As-dimer Chadi model [19]. (c) Arsenic-passivated Si surface with As dimers on neighboring terraces being mutually perpendicular. GaAs islands that form on each of the terraces are mutually rotated through 90° around a vertical axis. Island faceting by singular facets is shown.

netsky and Shklyaev [20] already back in 1979 that under certain annealing conditions two-atomic steps form on the silicon vicinal surface (001) → [110]. According to Bringans et al. [21], on the terraces of these steps Si–Si dimers have an identical orientation (Fig. 2a, *2*) — the so-called single-domain surface. For this reason, in the As monolayer deposited on the Si surface before GaAs starts to grow, arsenic dimers also have an identical orientation — either in the direction of Si substrate deflection (Fig. 2a, *3*) or along the step (Fig. 2a, *4*). Accordingly, after the onset of the Ga deposition, GaAs crystallites of one sign form on either of these two Si surfaces.

Other problems turned out to be more serious. Because of the film–substrate lattice mismatch (about 4% for the GaAs/Si system), GaAs films can have dislocation densities as high as 10^9-10^{10} cm^{-2}. The difference in the thermal expansion coefficients (6.63×10^{-6} K^{-1} for GaAs, and 2.3×10^{-6} K^{-1} for Si) also promotes the generation of a great quantity of dislocations and the nucleation of cracks in the GaAs film as the latter is cooled. There has only been mixed success so far in overcoming these problems. Figure 3 presents a classification scheme of methods for epitaxially growing GaAs on silicon substrates. All methods can be divided into two categories: direct growth on the Si substrate (left column), and growth using various buffer layers (right column). Historically (see above), the early experiments on GaAs-on-Si growth were performed by growing GaAs directly on Si. The basic techniques used for this purpose rely on lowering the density of threading dislocations (TDs) and are common to both GaAs/Si heterostructures and other heteropairs, such as Ge/Si and GaP/Si. The two most noteworthy techniques are thermal cycling [12, 13, 15] (Fig. 3a) and the employment of low temperatures and low GaAs growth rates at the initial stage, the so-called two-step growth [8, 22–29] (Fig. 3b). The first step refers either to producing several nanometers (or several dozen nanometers) of low-temperature-grown GaAs or to migration-enhanced epitaxy consisting of alternatively depositing Ga and As monolayers. Also categorized into the first step can be the solid-phase crystallization of a thin amorphous GaAs layer. Superthin layers of strained material (Si, InGaAs) inserted into the bulk of the GaAs layer actively initiate the annihilation of TDs, as do strained superlattices [10, 14, 30] (Fig. 3d).

Figure 4 (taken from work [15]) shows the dependence of TD density on the thickness of the GaAs layer in as-grown GaAs/Si films and those underwent thermal cycling. It is seen that four heating cycles up to 900 °C reduce TD density by an

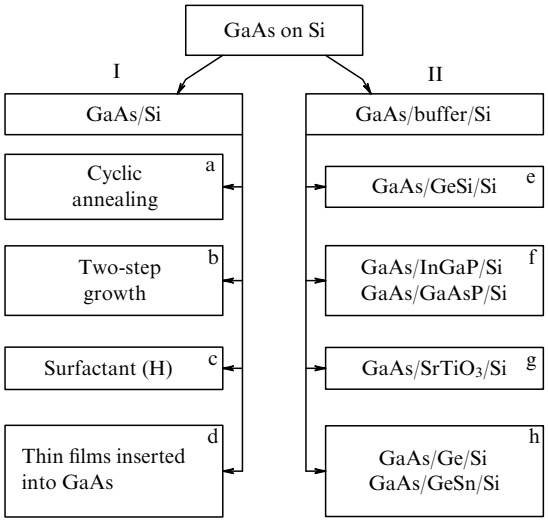

Figure 3. Classification of epitaxial GaAs-on-Si growth methods.

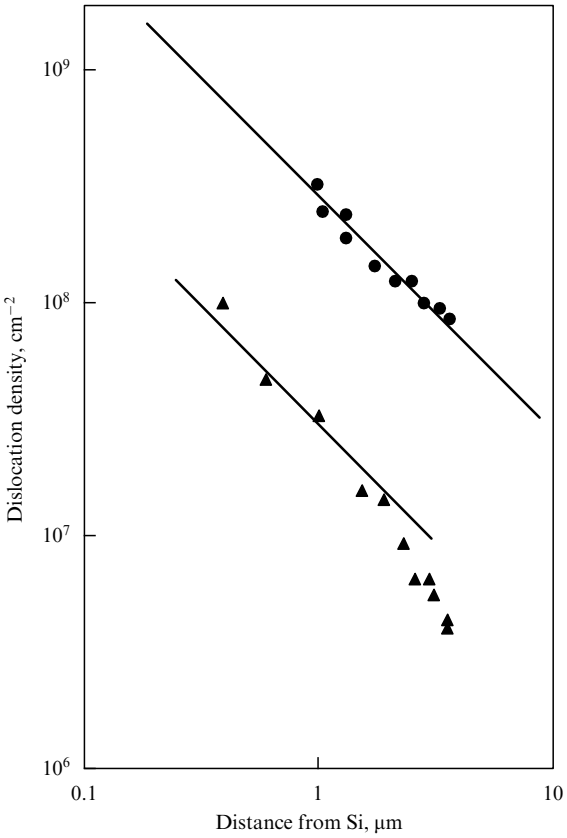

Figure 4. TD density vs. the thickness of GaAs film for an as-grown sample (●) and for a sample after four thermal cyclings from 900 °C to near-room temperature (▲) (taken from Ref. [15]).

order of magnitude; increasing the GaAs thickness h also decreases TD density (specifically as $1/h$).

Shown in Fig. 5 is the InGaP/GaAs/Si growth procedure of Ref. [26], which includes two-step GaAs growth (circumscribed by the dashed oval) followed by applying five heat treatment cycles to an as-grown GaAs film and subsequently growing an additional GaAs layer and the main InGaP layer. According to the authors of Ref. [26], this thermal cycling

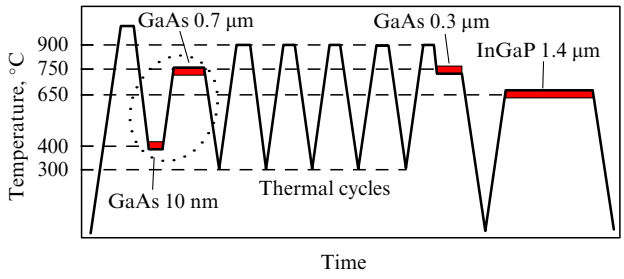

Figure 5. Succession of operations to grow the InGaP/GaAs/Si heterostructure using intermediate thermal cycles (taken from Ref. [26]).

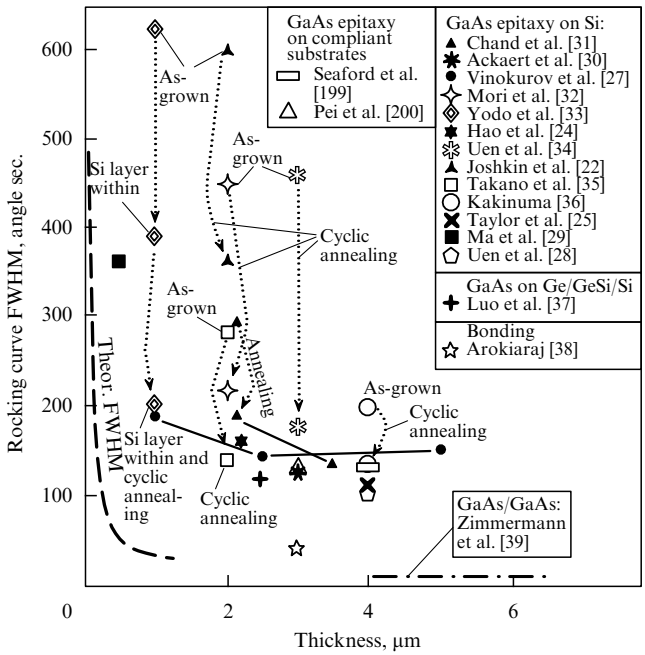

Figure 6. The full width at half maximum of the (004) X-ray rocking curve versus film thickness for GaAs film on Si substrate as given by various authors.

treatment caused an increase by a factor of 100 in the InGaP layer photoluminescence intensity. What makes thermal cycling so effective is that, because of the large difference between the thermal conductivity coefficients of the GaAs and substrate, a GaAs film subjected to large temperature oscillations will periodically switch between the compressed and extended states, thus reversing the motion of TDs. When encountering one another in various combinations, TDs with opposite Burgers vectors actively annihilate. However, as seen from Fig. 5, the upper temperature to which heterostructures are exposed is too high, which is not justified unless the annealed layer serves only as a platform for further film growth at lower temperatures.

The general structural quality of GaAs films grown directly on Si(001) can be assessed using X-ray rocking curves for a (004) plane reflection. The full width at half maximum (FWHM) of the reflection peak (the rocking curve full width at half maximum) depends directly on the concentration of defects in the film. Figure 6 summarizes available experimental data on the rocking curve full width at half maximum for GaAs films grown directly on an Si(001) substrate. It is seen that a wide variety of FWHM values corresponds to GaAs films with the same thickness. The

dotted downward arrows indicate a significant improvement in the structural characteristics of these films after thermal cycling or annealing treatment [22, 31–36]. Inserting a layer with a different lattice constant (Si [33], InGaAs [35]) also causes a decrease in the rocking curve FWHM.

Also shown in Fig. 6 (by a dashed line) is the theoretical dependence of the rocking curve FWHM on film thickness for a perfect (dislocation-free) film; the decrease in FWHM is due only to the fact that a perfect crystal has more reflecting planes. Epitaxial GaAs films grown by various techniques onto an Si substrate are prevented from approaching this behavior by their lack of structural perfection: it is only at the stage of separate nuclei where they can become pseudomorphic. Once a GaAs film starts to plastically relax — a process which involves the formation of a large number of defects in the near-substrate region — the rocking curve of the film cannot be close to its theoretical counterpart, as illustrated in Fig. 6. For the purpose of comparison, Fig. 6 gives the FWHM value (taken from Luo et al. [37]) of the rocking curve for a 2.5-μm-thick GaAs film grown on an Si substrate on top of a Ge/GeSi buffer layer. This value (equal to 120″) is the lowest to date for a GaAs film of this thickness epitaxially grown on an Si substrate. In the GaAs/Ge/GeSi/Si heterostructure, dislocations responsible for compensation for the GaAs–Si lattice mismatch are mainly concentrated within the GeSi buffer layer and have little or no broadening effect on the GaAs-film X-ray rocking curve.

There exist nonepitaxial methods for organizing a thin GaAs film on an Si substrate. In one of these, known as wafer bonding, a GaAs film grown on a GaAs substrate is detached from the latter and carried over to an Si substrate (for more on such techniques see Section 7). Unlike heteroepitaxy, where defects unavoidably occur in the film, in this case they are absent, and the rocking curve FWHM is determined by the imperfections that develop as GaAs/GaAs is homoepitaxially grown and wafer-bonded to the Si substrate. Arokiaraj et al. [38] were able to obtain a rocking curve FWHM of 44″ for a 3 μm thick GaAs film by bonding the film to an Si substrate and then selectively etching off the GaAs substrate (see Fig. 6). This value is the lowest one obtained for any several-micron-thick GaAs film and approaches the FWHM value recorded for thick homoepitaxial GaAs films (Zimmermann et al. [39], for example, report a rocking curve FWHM of 12″ for GaAs/GaAs, as shown by the dash-and-dot line in Fig. 6).

3. Direct GaAs-on-Si epitaxy

The 4% lattice mismatch between GaAs and Si is a significant obstacle to growing perfect GaAs films. The initial nucleation stages of GaAs on an Si substrate are key in this context and to a large extent determine the properties of a 'thick' GaAs film. Details of how one material nucleates on another of different crystallographic properties were the subject of intense study until 2000. The basic keys to understanding the early stages of GaAs-on-Si epitaxy are briefly outlined below.

3.1 Nucleation and 'islanding' mechanisms for heteroepitaxial films

The early studies [40, 41] showed that GaAs-on-Si nucleation occurs in the form of islands. The classical picture distinguishes three early film growth mechanisms (see, for example, Ref. [42]): layer-by-layer growth (Frank–van-der-Merve, or FM, mechanism), islanding growth alone (Volmer–Weber, or VW, mechanism); and the Stranski–Krastanov (SK) mechanism (an initially continuous film becomes islanded, but with a thin continuous 'wetting' layer left). In wetting–nonwetting terms, the first two mechanisms can be distinguished based on how the surface energies of the substrate (γ_s), the film (γ_f), and their interface (γ_i) interrelate. If the substrate surface energy is large enough to exceed the sum of the two others, the wetting regime occurs (the absence of open substrate surface is energetically favorable — the FM mechanism):

$$\gamma_s > \gamma_f + \gamma_i \,, \tag{1}$$

whereas the reverse inequality

$$\gamma_s < \gamma_f + \gamma_i \tag{2}$$

implies the lack of wetting (VM mechanism).

The SK mechanism was discussed by its authors [43] theoretically in studying the growth of lattice-matched films. Within the wetting–nonwetting framework, this mechanism can only come into play if we assume that the surface energies involved are related by inequality (1) early in the growth process but switch to inequality (2) after several monolayers (MLs) have been grown.

The SK mechanism as a characteristic of morphological transformation in a film growth was invoked in connection with the experimentally examined change from the two-dimensional (2D) to the three-dimensional (3D) growth mechanism in stressed GeSi/Si and InGaAs/GaAs films. It was found that in either case three-dimensional islands formed over the thin continuous wetting layer — hence, the adjective SK is often applied to this transition (see, for example, Refs [44, 45]). Detailed experimental and theoretical studies revealed, however, that (1) the driving force behind this transition is the fact that three-dimensional features have lower elastic deformations than continuous films (the system's free energy decreases due to elastic deformations being reduced near the tops of the three-dimensional relief [46]), and (2) that the mechanism by which this transition occurs is the surface migration of adatoms. This mechanism (known as the ATG mechanism) was theoretically proposed by Azaro and Tiller [47] and Grinfel'd [48] and can be found discussed in detail in the comprehensive review by Politi et al. [49].

The spontaneous formation of high-density islands has found current practical applications in the heteroepitaxy of high-stress structures — Ge-on-Si and InAs-on-GaAs nanoislands (see, for example, reviews [50, 51]). The presence of a wetting layer (3–4 ML for Ge/Si [52, 53] and $\sim$ 1.5–1.7 ML for InAs/GaAs [54]) in these two types of heterostructures suggests that the change in the interrelation of the surface energies [leading to a change from Eqn (1) to Eqn (2)] also occurs at the early stages of the epitaxy of highly stressed films in Ge/Si and InAs/GaAs systems. Thus, there are in fact two island-creating physical factors behind the common term 'Stranski–Krastanov mechanism': the decrease in the elastic deformation energy in 3D islands due to their elastic relaxation, and the change in the substrate surface energy due to an absorbate coming to the surface (Ge on Si or InAs on Si). The first factor is the driving force which acts both at the microlevel (nanometers)

and at the macrolevel (fractions of a micron, including initially continuous films with thicknesses ranging from dozens to hundreds of nanometers). The second factor operates within a few monolayers of the new deposit at the initial stage of heteroepitaxy.

GaAs-on-Si epitaxy involves no wetting layer [40, 41]; GaAs islands form directly on the substrate and, hence, the initial growth mechanism of this heteropair is VW, in which the 'islanding' of the film occurs because of the energetic favorability of a free substrate surface. However, in this case the free energy of the forming 3D features also decreases due to the decrease in elastic deformations at the island tops — implying the operation of the ATG mechanism [47, 48]. Thus, at the early stages of GaAs-on-Si growth the single term 'Volmer – Weber mechanism' again implies two island-forming physical factors: a decrease in the energy of elastic deformations in 3D islands due to their elastic relaxation, and the energetic unfavorability of the continuous wetting of the Si substrate by GaAs absorbate [see inequality (2)].

Adomi et al. [55] demonstrated the central role the decrease in the substrate surface energy has in the GaAs-on-Si growth process. They showed that when GaAs is to be grown on a Si film which is preliminarily grown onto a bulk GaAs substrate and is pseudomorphic (i.e., lattice-matched to GaAs) with a thickness of 0.9 nm, then GaAs growth also initially occurs by the island mechanism. Presumably, the reduced chemical activity of the arsenic- or gallium-passivated Si surface contributes heavily to the onset of the 3D GaAs/Si growth mechanism at the initial stage of epitaxy. A confirmation also comes from GaP-on-Si growth, where the lattice mismatch is much lower (0.37%). GaP/Si is also a system where islanding growth at the initial stage is a major problem (for more on this see Section 5).

3.2 Initial stages of GaAs growth on Si

Realization that passivating an Si surface by group III or V elements — the necessary condition for growing semiconducting III – V compounds on Si — results in the islanding growth of GaAs in the initial stage of epitaxy led to a wide diversity of approaches to depositing GaAs (and also GaP) onto Si. These include: the use of an epitaxial substrate, i.e., the preliminary deposition of an Si epilayer on Si [23, 32, 56, 57]; low-temperature growth of the first several dozen or hundred GaAs [22, 27, 32, 58 – 60] or GaP [61 – 63] monolayers; the migration-enhanced epitaxy of Ga and As alternately [25, 60, 64 – 66], and the growth of 'amorphous' Si and GaAs layers [24, 28, 58]. So far, the most widely used technique — the so-called two-step growth — involves the low-temperature (400 °C) growth of GaAs in the initial stage followed by annealing and by growing the main part of the GaAs film at about 550 – 600 °C, the typical temperature for this compound. The idea of this particular order of growth is that at low growth temperatures the deposited GaAs layer should be continuous before structural defects are introduced.

Let us look at this in more detail. At the very initial stage of growth, the height of a GaAs/Si island relates to its lateral size in the substrate plane as 1/2 [16, 56, 67, 68]. Note, for comparison, that at the early formation stages of Ge-on-Si(001) islands the lateral walls of the islands are {105} faces and the ratio of the height to the lateral size is 1/10. That the aspect ratio of GaAs/Si islands is much greater than analogous ratio for Ge/Si indicates that the formation of 3D GaAs islands on Si is more favorable energetically.

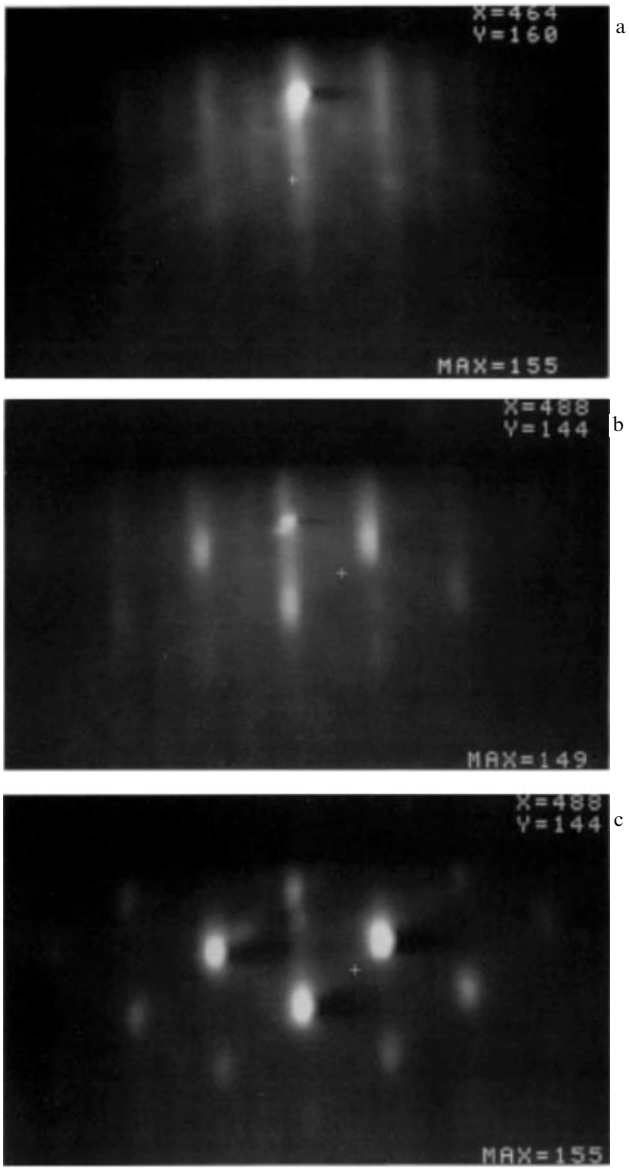

Figure 7. RHEED patterns for an Si substrate surface when clean and after GaAs deposition at the initial stage of GaAs/Si epitaxy. (a) Si surface; (b, c) average GaAs thickness of 0.14 nm and 0.28 nm, respectively. Si substrate deflected: (001) → [011]. GaAs deposition temperature 400 °C. (Taken from Ref. [56].)

According to Asai et al. [56], even after the deposition of a GaAs layer with an average thickness of 1 ML (Fig. 7b) and let alone 2 ML (Fig. 7c) onto Si the reflections on RHEED patterns turned out to be pointlike, indicating the onset of the islanding mechanism. An atomic-force microscopy study revealed the formation on this surface of hemispherically shaped ($h/l \sim 1/2$) islands at a density of about 10^{11} cm^{-2}. A further increase in the average thickness of the GaAs layer has little effect on the shapes of the islands, which can be seen in the cross sections of these structures, as presented by Fang et al. [16] and Tsai and Kao [67], and in atomic-force microscopy surface images [56, 57]. Figure 8 depicts a microphotograph taken from Usui et al. [68] that shows the cross section image of GaAs islands on Si. Seen in the figure are islands that formed after the deposition of four MLs of GaAs at a temperature of 400 °C and which are hemispherically shaped and dislocated.

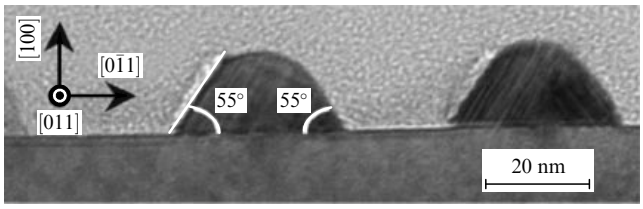

Figure 8. Electron microscope cross section image after the deposition of four GaAs monolayers onto an Si substrate. Temperature 400 °C. (Courtesy of the authors of Ref. [68].)

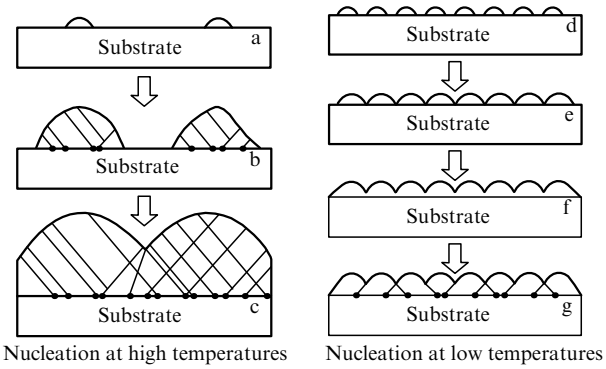

Figure 9. Two approaches to introducing misfit dislocations. Left: dislocations and other structural defects are introduced before the islands coalesce. Right: MDs are introduced into a continuous pseudomorphic film.

According to LeGoues et al. [69], who monitored the growth of Ge islands on an Si substrate *in situ* with an electron microscope, dislocations nucleate in higher-stress regions near island edges; this behavior has also been observed by other authors [70–72]. What this means is that a GaAs island on an Si surface can be thought of as hemispherical. As noted in Refs [73, 74] based on stress and deformation calculations for such initially pseudomorphic islands, the island–substrate interface is distorted, and it is on the island edges where stresses concentrate and misfit dislocations (MDs) and other defects are most likely to nucleate. As early as 1975, Stowell [75] described in detail how the coalescence of dislocated 3D islands at the initial stage of film deposition can lead to a large density of TDs in a thick epitaxial layer. Hence, there is a desire on the part of researchers to create such growth conditions for stressed films under which the first MDs would be introduced into an already continuous film.

The lower the initial growth temperature, the smaller the region where adatoms can (diffusively) assemble themselves into an island, and hence the higher their density. In accordance with this understanding, Fig. 9 presents two ways in which a GaAs layer can develop via the coalescence of islands: one for high, and the other for low temperatures. At the standard GaAs growth temperature of 550 to 600 °C and, as seen in Fig. 8, at 400 °C, GaAs islands become defective even before they coalesce (on the left of the diagram, Fig. 9b). When such islands coalesce (Fig. 9c), immobile (trapped) defects form in large numbers, which are difficult to remove by subsequent operations like annealing, the growth of higher-thickness layers, etc.

If pseudomorphic GaAs islands coalesce in the way shown in Figs 9e and f, then the rough surface becomes a source of defects, and these are now introduced into a continuous GaAs film (Fig. 9g). Because the island density in this case is at least an order of magnitude higher than for the high-temperature case, it follows that the defects generated by this surface (Fig. 9f, g) should also be higher in density. There is solid experimental evidence, however, that using the low-temperature approach at the initial stage of epitaxial GaAs growth is beneficial in the sense of reducing the rocking curve FWHM, implying the improved structural perfection of these films. How can this be explained? One possible answer is that the defects introduced into the continuous GaAs film may form a less diverse and, as a whole, more mobile set; so that as growth procedures continue, many of the defects may annihilate.

In the work by Taylor et al. [25], who used a combination of ultralow deposition temperature (75 °C) with migration-enhanced epitaxy, the GaAs film had a thickness of 80 nm. The authors note that GaAs grown at this temperature was fully relaxed and single-crystalline judging from the presence of long line-shaped RHEED reflections spaced by a distance characteristic of unstressed GaAs. The measured X-ray rocking curve FWHM of a 4-μm-thick GaAs film amounted to 110″ (see Fig. 6). A point is made of the fact that the growth process employed did not involve intermediate high-temperature annealing — a treatment which substantially improves the crystal properties of GaAs but cannot be used to manufacture complex device structures.

To our knowledge, no detailed nanolevel studies of early GaAs/Si growth stages as a function of temperature have been conducted, in which the researchers have been able to observe the change from islanding growth to a continuous GaAs film. There is one point to note, though. In one of the early studies on the subject [40], a continuous GaAs layer about 20 nm thick was observed at 225 °C. As the deposition temperature was increased for the same average thickness, the GaAs film was island-like. The islands decreased in density from $\sim 2 \times 10^{11}$ cm^{-2} (300 °C) to $\sim 10^{10}$ cm^{-2} (600 °C), while at the same time growing in size. Lower-thickness films of deposited GaAs were not investigated in that study. Tachikawa et al. [23] report that 10-nm-thick GaAs films grown at 400 °C were continuous. This is meager data from which to determine at what epitaxial growth temperature, if at all, GaAs islands coalesce when pseudomorphic, so the diagram in Fig. 9 we considered earlier is just a speculation.

Let us now turn to the use of ultralow temperatures and of amorphous GaAs and Si layers. As early as 1988, Castagné et al. [76] showed that 350 °C annealing following GaAs deposition in the form of an amorphous nonstoichiometric deposit with an equivalent thickness of ~ 1.5 nm leads to the solid-phase crystallization of GaAs, and that three-dimensional surface morphology is not observed. In a study by Soutadé et al. [58], each of three GaAs monolayers was deposited at ambient, presumably near-room, temperature at which As and Ga form a kind of a mixture which the authors call amorphous GaAs. The RHEED patterns following heating at 400 °C reveal the absence of islands and the presence of a continuous GaAs layer. The relaxation rate as determined from the change in the screen distance between the selected reflections was considerably slower than in the standard regime (Fig. 10). It can be hypothesized that the solid-phase crystallization of each of the three GaAs layers — the process initialized on the side of the substrate — occurred in the 2D regime because the amorphous GaAs fraction present on top of the material being crystallized prevented atoms from diffusing along — and hence hindered

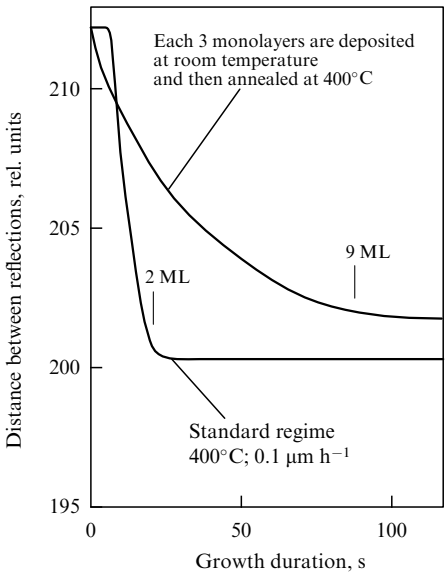

Figure 10. Change in distance between RHEED reflections (azimuth ⟨001⟩) at the initial stage of GaAs-on-Si deposition. Arrows tie the number of deposited GaAs monolayers to the growth duration. (Taken from Ref. [58].)

the 'islanding' of — the surface of the film being crystallized. Another possibility is that the amorphous state of the film (and the substrate) enables GaAs, in the solid-phase crystallization process, to rapidly switch to a plastically relaxed state, namely, to a crystallized state with built-in defects. However, for a low-thickness film, after GaAs becomes single-crystalline and the stresses due to the lattice parameter mismatch are not fully relieved, it should be expected that, due to the ATG mechanism [47, 48], such a film will again tend to 'islanding', with its crystal structure correspondingly deteriorated due to introduced defects. Therefore, the initial deposition thickness of the amorphous layer of the crystallizing material should considerably exceed the critical thickness for the onset of plastic relaxation, which is about 1 nm for the GaAs/Si(001) system in question. This condition was satisfied conservatively in the studies reviewed below.

It was noticed as early as 1991 by Vinokurov and coworkers [27] that an amorphous inset made early in the GaAs/Si growth process greatly improved the structural perfection of GaAs films. GaAs/Si layers were grown using the MOSVD hydride process. At the initial stage, the substrate was coated with a thin (40 nm or less) layer of amorphous GaAs, which was subsequently recrystallized at 750 °C. Following this, a standard technique was applied to grow GaAs films up to 5 μm thick. Referring to Fig. 6, it is seen that these films have their X-ray rocking curve FWHM values located at the lower part of the body of experimental data.

Uen et al. [28] reported that a 4-μm-thick GaAs film grown by metal-organic vapor-phase epitaxy (MOVPE) using an amorphous layer of Si (2 nm) and GaAs (25 nm) at the initial stage of epitaxial buildup had a rocking curve FWHM of 102″, the best result for a GaAs film of this thickness (see Fig. 6). It should be noted that the growth process used by the team involved high-temperature annealing (thermal cycling between 780 and 200 °C) both after the growth of amorphous layers and in the interval preceding the deposition of the main GaAs layer, which somewhat compromises the use of amorphous layers.

As the studies reviewed [27, 28, 58] suggest, the initial introduction of amorphous and 'ultra-low-temperature' Si and GaAs layers followed by their solid-state crystallization improves the structural properties of the main GaAs film; however, further studies are needed to understand the mechanism of how such layers affect the course of GaAs plastic relaxation.

3.3 Atomic hydrogen-assisted GaAs/Si growth

Molecular beam epitaxy and other current epitaxial technologies (chemical vapor deposition with dissociation of the SiH_4 and GeH_4 compounds near the substrate; gas-source MBE with gaseous Ge, Si, III–V compounds, etc.) primarily use atomic hydrogen to clean the substrate surface before growth, as well as a surfactant that affects the building-in of adatoms. Fundamental aspects of the hydrogenized surfaces of III–V compounds are summarized in a recent review [77]. The substrate cleaning process is abundantly described in the literature [79–82] and relies on the desorption of oxygen and carbon due to the formation of their volatile compounds following chemical reactions involving hydrogen radicals [78]. As shown by many authors, using atomic hydrogen in the MBE process slows down the 'islanding' mechanism [83, 84], smooths out heterointerfaces [85, 86], and reduces the segregation (floating-up) effect for Ge and Sb dopants (if used) during GeSi-on-Si growth [87–89]. It is conjectured that the role of atomic hydrogen in epitaxial deposition of films is due to the reduced diffusion length for adatoms moving along the surface [85, 90]. For example, it is shown in Ref. [91] that in the presence of atomic hydrogen the density of two-dimensional nuclei of Ge on Si(111) increases by an order of magnitude, indicating the surface migration of Ge adatoms to be passivated.

While the beneficial effect of atomic hydrogen on the epitaxial growth of stressed films has been observed many times in Ge/Si and InAs/GaAs heterosystems, virtually no studies are available on the role of atomic hydrogen in the GaAs/Si system. In this context, it is worthwhile to mention the first demonstration, in the 1993 study by Okada et al. [92], of the improved properties of a GaAs layer grown on an Si substrate with the continuous participation of atomic hydrogen. In that study, under certain experimental conditions the density of TDs decreased from 10^8 cm^{-2} to $\sim 10^5$ cm^{-2}, but the initial epitaxy of GaAs on Si in the presence of atomic hydrogen was not studied, nor indeed were we able to find any follow-up studies by even the same team. While the 2004 study of Ref. [93], also coauthored by Okada, was concerned with the growth of GaAs on Si, it used atomic hydrogen only in preparing GaAs film by MBE on a GaAs/Si platform preliminary grown by MOVPE without using hydrogen.

4. GaAs-on-Si growth through buffer layers

When relying on high-temperature heating, a technique for growing perfect GaAs/Si layers does not always meet requirements which are placed on the whole of the heterostructure, with its preliminary grown layers differing in thickness, doping size and type, and which demand that subsequent temperatures not exceed a certain limit. For this reason efforts have also been made to develop such methods for obtaining GaAs on a dissimilar substrate, which would enable GaAs films to be grown with standard GaAs-on-GaAs processes. The basic idea of these methods is to place between GaAs and the Si substrate the layers of other materials, with

their lattice constants and thermal expansion coefficients lying in-between. Such materials are listed in Fig. 3 (right column, e to h).

The most well-developed method of preparing an artificial substrate is that using the Ge/GeSi/Si heterostructure. As seen in Fig. 1, GaAs and Ge have close values of the lattice constant. Early studies on the growth of perfect GaAs-on-Ge films showed that the main imperfections present were antistructural defects and antiphase boundaries [94, 95], whose density was reduced to zero by deflecting the substrate through a few degrees with respect to (001) orientation [96–98]. It was therefore logical to try to grow GaAs on Si through buffer layers having pure Ge on their surfaces.

4.1 Artificial Ge/GeSi/Si substrate as a platform for growing GaAs

Fabrication of a buffer layer with a varying lattice constant and a stepwise or linearly growing content of a new solid solution component is a long-known and widely used method of preparing GaAsP/GaAs heterostructures. Pioneering works along these lines date back to as early as the late 1960s [99, 100]. In the 1990s, Fitzgerald and his coworkers [101–105] studied in detail the growth of GeSi solid solutions of variable composition on Si substrates and, as of today, perfect GaAs platforms on Si(001) substrates are primarily prepared by growing GaAs films on Ge, the latter of which, in turn, is grown on Si(001) through a graded GeSi buffer layer. Because the Ge/GeSi/Si(001) heterostructures are independently and widely used, a detailed discussion of how they are grown is in order.

The fundamental 1991 study by Fitzgerald et al. [101] on fabricating GeSi buffer layers on Si reported the growth of Ge_xSi_{1-x}/Si(001) films with $x \lesssim 0.5$ and a TD density of no more than 2×10^6 cm^{-2}. It was already then that the following problems arose: preparing GeSi films with this TD density requires that the Ge portion increase throughout the depth may not be more than 10% per micron of the buffer layer thickness. This meant a high material consumption and necessitated using high growth temperatures ($\sim 900\,^\circ$C) to make the HS growth cycle acceptable in terms of duration. The high growth temperature, in turn, led to a higher (up to hundreds of nanometers) roughness of the final product's surface [102].

The problem of surface roughness was solved in part by using Si substrates deflected by a few degrees with respect to the exact (001) orientation, and by chemically polishing the surface of the film [103]. In addition, the composition of the graded Ge_xSi_{1-x} layer was brought to $x = 1$, thus achieving the goal of growing a 100% Ge film. By chemically polishing the Ge_xSi_{1-x}/Si(001) HS at the intermediate stage with $x = 0.5$ and subsequently allowing the GeSi buffer layer to grow to become pure Ge, the authors of Ref. [104] demonstrated the possibility of obtaining an artificial Ge/GeSi/Si(001) substrate with a TD density of no more than 2×10^6 cm^{-2} in the Ge layer. Lee et al. [105] documented the basic achievements made with this technique (by 2005) in fabricating field-effect transistors (FETs) based on stressed Si, GeSi, and Ge channels. The device applications of this platform also include germanium photodiodes [104] and AlGaAs lasers [106]. Figure 11 displays an electron microscope image of the cross section of the laser heterostructure AlGaAs/GaAs grown on a Ge/GeSi/Si platform fabricated with the technology described in Ref. [103]. Seen in the figure is that part of the graded GeSi layer hosting MDs necessary

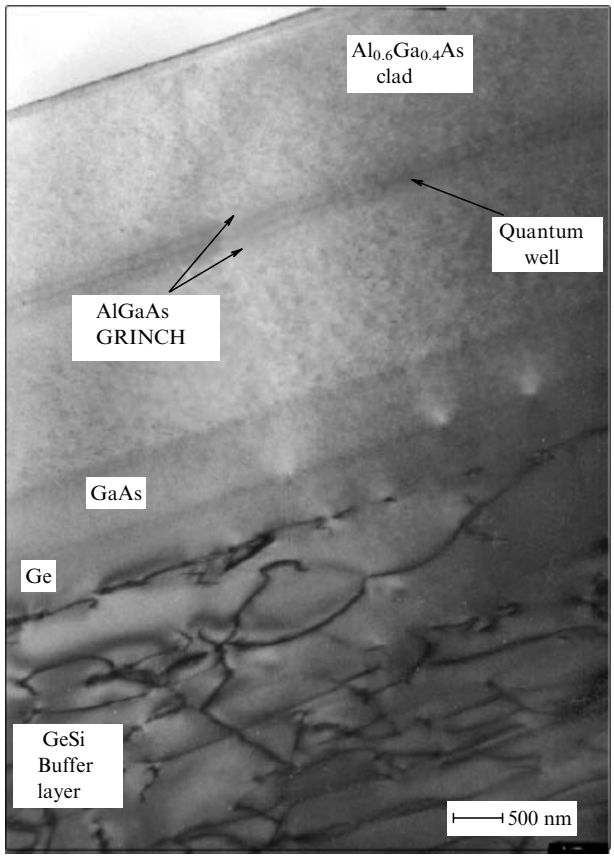

Figure 11. Cross section micrograph of laser heterostructure AlGaAs/GaAs grown on a Ge/GeSi/Si platform. (Courtesy of the authors of Ref. [106].)

for creating a smooth unstressed changeover, both in terms of the lattice constant and the thermal expansion coefficient. To smooth out the surface of the growing film, intermediate chemical–mechanical polishing of the surface was carried out at the $Ge_{0.5}Si_{0.5}$ stage. The laser heterostructure based on AlGaAs with quantum wells was grown by MOVPE.

Other methods of growing graded buffer layers of GeSi on Si(001) substrates were developed in parallel [107–117]. The most noteworthy of these is low-energy plasma-enhanced chemical vapor deposition (LEPECVD) of Si, Ge, and GeSi [111–117]. The advantages of this technology include a high growth rate (up to 4–5 nm s^{-1}), lower growth temperatures ($\sim 550\,^\circ$C), and the fact that the GeSi composition depends virtually linearly on the ratio of the components (SiH_4/GeH_4) introduced into the reactor. The density of TDs in Ge/Si films was lowered to 1×10^5 cm^{-2}, which the authors of Ref. [114] claim is lower by a factor of 4 to 10 than previously known. The main advantages of this technique over the competing technique of reduced pressure-chemical vapor deposition (RP-CVD) are reviewed in Ref. [115]. Because of the lower growth temperature of GeSi layers and possibly due to the surface smoothing effect of atomic hydrogen, which may, following the dissociation of hydrogen molecules in the plasma, be present on the surface of the growing film [84, 90], GeSi and Ge/GeSi/Si films grown by LEPECVD have much lower surface roughness compared to other technologies. Figure 12 presents the root-mean-square (rms) roughness values of the surfaces of graded GeSi layers grown with various techniques. Hartmann et al. [108]

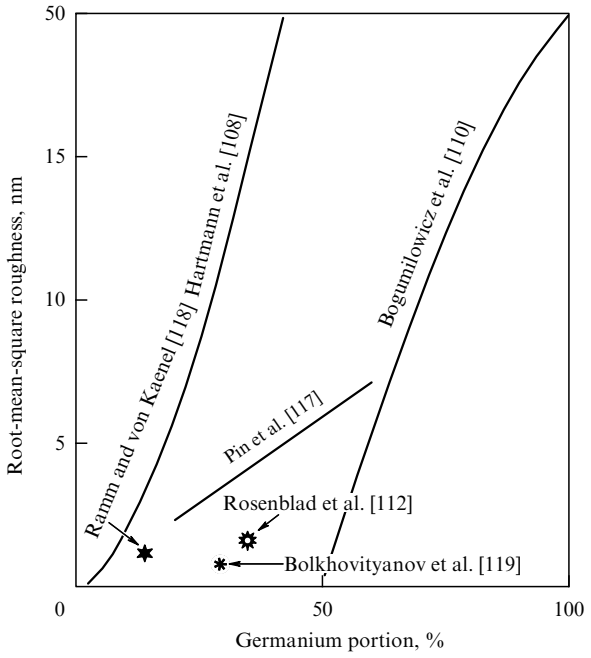

Figure 12. Root-mean-square roughness of the surfaces of plastically relaxed GeSi/Si(001) films versus Ge percentage (as given by various authors).

produced graded GeSi layers using gas-source molecular beam epitaxy (GS-MBE). Despite the low growth temperature (550 °C), the roughness of layer surfaces increases dramatically with Ge percentage, differing little from the values characteristic of chemical vapor deposition (CVD) with its high growth temperatures (~ 900 °C). Bogumilowicz et al. [110], using RP-CVD technique and high growth temperatures (850 °C), applied an intermediate chemical polishing procedure to the surface of a GeSi layer grown to 50% Ge portion (the same as done by Samavedam et al. [104]). As seen in Fig. 12, the surface roughness of GeSi films grown on this platform increased dramatically for a Ge content higher than 50%. At the same time, GeSi films grown by low-energy plasma-enhanced chemical vapor deposition have much lower surface roughness; in Fig. 12 this is illustrated by data points taken from the research studies by Ramm and von Kaenel [118] and Rosenblad et al. [112], and by the dependence from Pin et al. [117] that characterizes mass industrial production. Notice the very low surface roughness of GeSi/Si(001) films having stepwise composition, which were grown using a smoothing surfactant Sb (see Bolkhovityanov et al. [119]).

Thus, as of now, a perfect Ge/GeSi/Si(001) platform to further grow GaAs and other semiconducting III–V compounds can be fabricated by a variety of industrial methods used to obtain GeSi films on silicon substrates. Immediately following the creation of the platform, activities on growing GaAs on such heterostructures began and basic GaAs parameters started to be investigated in comparison with GaAs films grown on GaAs and Ge substrates [120–125]. The device applications of these HSs are discussed below.

4.2 Graded GaAsP and InGaP layers

As seen in Fig. 1, another 'crystallographic pathway' for changing the lattice constant smoothly or step-by-step is traversed through GaP (arrow *b*) and further to GaAs through GaAsP [126–129] or InGaP [130] transition layers (arrows b_1 and b_2). In all cases, a thin GaP buffer layer should be grown at the initial stage of epitaxy. Despite the small (0.37%) GaP–Si lattice mismatch, GaP (similar to GaAs) nucleates by a 3D VW mechanism, making wetting a key problem. The initial stages of GaP-on-Si growth are taken up in more detail in Section 5.

In studies by Takagi et al. [127] and Tsuji et al. [128], short-period GaP- and GaAs-based superlattices with a gradually increasing content of GaAs were used as a transition layer. Figure 13 presents a schematic of how the lattice constant averaged over each superlattice packet varies with the thickness of the transition layer as used in Ref. [128]. As seen from the figure, the total thickness of the transition layer is close to 1 μm, which is 10 times smaller than for Ge/GeSi/Si. GaP and the transition layer GaAsP were grown by migration enhanced epitaxy. It is known [10, 16] that stressed superlattices considered as inserts (and it is to be noted that in this case the entire GaAsP transition layer consisted of superlattices) introduce additional stress fields that make the TDs faster to move and easier to annihilate. Based on their RHEED observations, the authors claim the entire epitaxy process to have occurred by a 2D growth mechanism. A point to note is that the epitaxial process used in this study involved atomic hydrogen, a fact which may have enhanced the stability of the 2D growth mechanism.

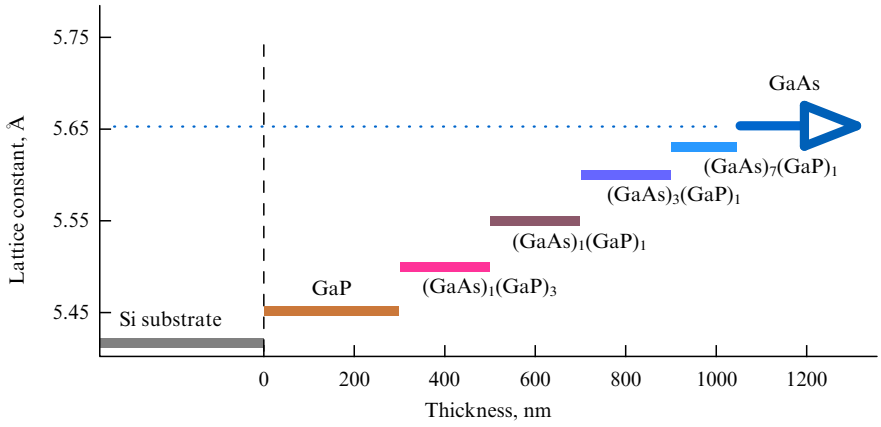

Figure 13. Stepwise-graded Si-to-GaAs transition formed by short-period superlattices of the $GaAs_mGaP_n$ type, where *m* and *n* are the numbers of bilayers. Each superlattice repeats itself until the thickness shown in the figure is achieved. (Taken from Ref. [128].)

In some cases, the lattice parameter of the buffer layer need not be varied to match that of GaAs. For example, Geisz et al. [129] used a GaAsP-based buffer layer with the variable composition to further grow HSs for solar cells consisting of three-component compounds of the $GaAs_{0.7}P_{0.3}$ and $Ga_{0.6}In_{0.4}P$ types, with the band gap lying between those of GaAs and GaP (see Fig. 1).

4.3 Buffer layers with the constant composition

4.3.1 GaAs/Ge/Si. In most cases, fabricating devices on Si substrates comprising GaAs layers requires that the distance (along the height) between the GaAs and Si surfaces be small. Therefore, reducing the transition layer thickness is a topical problem whose full solution has not yet been found. One possibility is to deposit a thin Ge layer onto an Si substrate, and then to grow GaAs onto this layer [131 – 134]. This approach overcomes the mismatch problem because GaAs and Ge are close in lattice constants and thermal expansion coefficients. In addition, GaAs-on-Ge nucleation occurs by a 2D mechanism (see, for example, Ref. [94]). There arises another problem, however, that lies in growing a perfect Ge layer of small thickness (~ 1 μm) on Si. The lattice mismatch in the Ge/Si pair is also $\sim 4\%$ (see Fig. 1), and there is a large mismatch between the linear thermal expansion coefficients: 5.92×10^{-6} and 2.3×10^{-6} K^{-1} for Ge and Si, respectively. A number of attempts to grow GaAs onto a thin Ge layer deposited on Si were made in the period before 1985, when the crystallization of Ge on Si was known in much less detail than now. It was observed, though, that introducing submicron-thick layers of Ge between Si and GaAs improved the properties of GaAs films [131 – 133].

The initial stages of Ge-on-Si(001) and -Si(111) growth processes have quite a long history of study because these combinations constitute two fundamental systems [together with InAs/GaAs(001)] which display the formation of islands with high densities — a phenomenon of key applied relevance to nanotechnology (see, for example, reviews [51, 135]). As is now well known, the initial Ge-on-Si growth is promoted by the SK mechanism, in which the Ge film is continuous up to a thickness of about 4 ML (see, for example, Eaglesham and Cerullo [136] and references cited therein). Beyond this thickness, Ge islands with a density of $10^{10} - 10^{11}$ cm^{-2} form, whose coalescence produces a large number ($\sim 10^{10}$ cm^{-2}) of defects that thread the Ge film [133]. The density of the threading dislocations can be significantly reduced by cyclically annealing the ready HS with an upper temperature limit of 900 °C [137, 138]. Similar to GaAs/Si, the efficiency of thermal cycling is due to the fact that, because of the wide range of temperature oscillations, the Ge film is intermittently stressed and stretched, with the result that a TD moves intermittently in one direction and in the opposite direction. TDs encounter each other in various combinations and actively annihilate one another. Note, however, that the upper limit for heating HSs is close to the Ge melting point (937 °C), which in most cases in unacceptable for growing complex compositions with preliminarily created p – n junctions.

There also exist various techniques that minimize the density of threading dislocations at the initial stage of epitaxial growth (first several dozen angströms). For a 4% lattice mismatch, the plastic relaxation of a Ge film starts at a very small thicknesses. To suppress or at least to decrease as much as possible the nucleation of TDs at the island coalescence stage, a number of passivation methods have been proposed for the changeover from layer-by-layer to islanding growth. The natural thing to do was to lower the Ge growth temperature at the initial stage, so as to slow down island formation kinetically. Experiments along this line were carried out at temperatures of 330 °C [139], 350 °C [137], and 370 °C [140], but it was found that continuous layers of Ge/Si(001) grown at low temperatures again showed a tendency to 'islanding' and increased defect production as the temperature was increased. For example, Halbwax et al. [139] showed that the Ge films grown at low temperatures are unstable within a thickness of 27 nm. Despite the fact that relaxation is already practically complete at an average thickness of 7.5 nm, a considerably large thickness is needed to secure two-dimensional growth at 600 °C.

Another possible way to suppress the islanding growth of Ge has to do with the effect of surface-active impurities (surfactants) on the stabilization of layer-by-layer growth in the Ge/Si system. In fact, with the use of surfactants such as arsenic, antimony, and atomic hydrogen for growing Ge on Si(001) substrates, two-dimensional growth of films continues at thicknesses larger than 4 ML of Ge [141 – 145]. This fact, however, cannot prevent the formation later on of a rough Ge film surface due to the ATG mechanism [47, 48], i.e., due to the appearance of elastic relaxation via the formation of a 3D surface relief. As reported by Horn-von Hoegen et al. [146], with the use of Sb as a surfactant, even though the Ge film remains continuous, its roughness increases, and for an average coating of about 12 ML of Ge, defects of high densities are introduced. Attempts to use surfactants for growing perfect Ge films with thicknesses of no more than 1 μm on Si(001) substrates also have thus far met with no success.

Positive results were achieved in the system Ge/Si(111):Sb (see, for example, Ref. [147] and references cited therein), i.e., when Si substrates of the (111) orientation were employed. As shown in Refs [148, 149], in this case an ordered network of misfit dislocations forms at the interface; these dislocations are of the edge type, i.e., the most favorable energetically. According to the studies' authors, the formation mechanism of such a dislocation network is that mobile dislocations nucleating on the rough surface of a still thin film (8 or more Ge monolayers [150, 151]) slide over the inclined {111} planes towards the interface which also is a glide plane for them. As a result, interaction between dislocations becomes easier and it is this interaction which leads to the formation of an ordered network of edge misfit dislocations at the interface and owing to which the threading segments (which the authors believe actively annihilate) have an ultimate density of no more than 10^8 cm^{-2} [150].

This, as seen from the analysis of plastic relaxation mechanisms in the system Ge/Si(111), necessitates that an ordered network of edge type misfit dislocations form at the initial stage of plastic relaxation. It seems that the factors favoring this in the Ge/Si(111) system are both the higher step formation energy on {111} planes compared to {001} planes [152] (which hinders the formation of surface roughness, while favoring the formation of extended islands with flat tops), and the possibility for the dislocations to slide along the interface. The {001} surface does not have such advantages, and despite the employment of surfactants [146, 153, 154], attempts to grow thin (~ 1 μm) perfect Ge films on the substrates of this orientation — the ones most widely used in semiconductor technology — were unsuccessful until 2005.

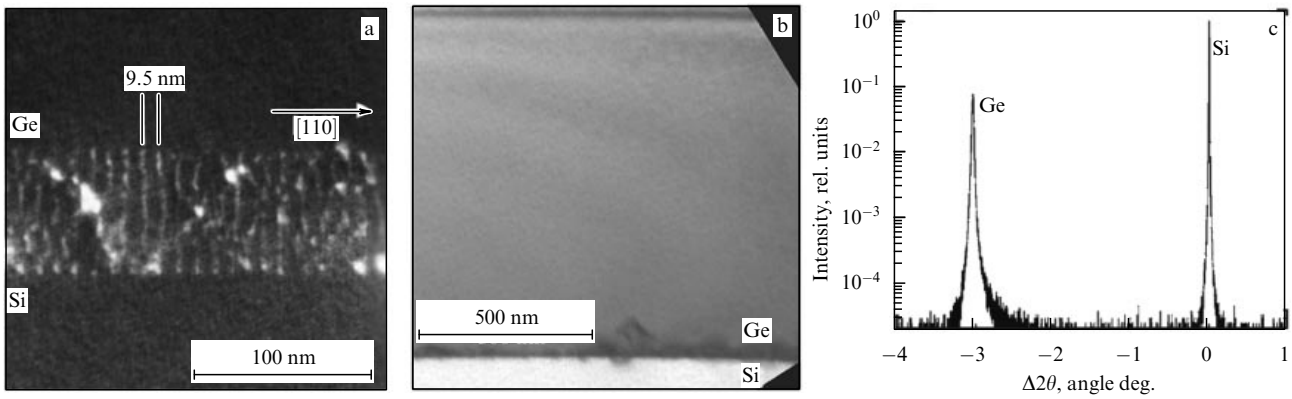

Figure 14. (a) Weak-beam dark-field electron microscope images of heterointerface Ge/Si(001) tilted by 25° around the [110] axis. (b) Bright field image of the cross section of a 1-μm-thick Ge film grown on Si(001). (c) (004) X-ray rocking curves for 1-μm-thick Ge film grown on Si(001). (Courtesy of the authors of Refs [155, 156].)

The 2005 – 2006 studies by Wietler and coworkers [155, 156] demonstrated the growth of submicron-thick perfect Ge films on Si(001) substrates. At the interface, an ordered dense network of misfit dislocations was reported to be observed (Fig. 14a, b). Judging from Fig. 14c, the FWHM of the Ge film X-ray rocking curve was at the level of 100″, which is a record value for submicron-thick Ge films grown directly on Si(001) substrates.

The key differences in this study compared to previous ones were the increase to 700 °C in the Ge-on-Si(001) growth temperature and the use of a continuous Sb flow throughout the entire duration of the growth. The last measure was a forced one necessitated by the fact that at this temperature antimony actively re-evaporates from the surface: the continuous flow enables Sb to continue to act as a 2D → 3D passivating element. It can be conjectured that also in this case, due to the elevated film growth temperature, the mechanisms responsible for the nucleation of complementary dislocations and those determining the formation of the ordered network of edge misfit dislocations became the key factors determining early plastic relaxation, and that the appearance, due to surface islanding, of defects of various complexity was slowed down by the presence of the surface-active Sb impurity. On such a platform, it is possible to grow perfect GaAs films.

Recently, one further approach has been proposed for growing thin perfect Ge films on Si(001) substrates. Bauer at al. [157] used chemical vapor deposition involving deuterium-stabilized tin hydrides to grow GeSn films with a few percent tin content. Bauer and his coworkers claimed — and this was later confirmed in Refs [158, 159] — that even films with a thickness of less than 100 nm are practically completely relaxed, their surfaces are atomically smooth, and the lattice constant mismatch is compensated for by edge dislocations located close to the film – substrate interface. The defect density in Ge films reached $\sim 10^6$ cm^{-2}, and the (004) X-ray rocking curve FWHM for Ge layers was typically 0.07°. Moreover, a GaAs layer was grown onto the GeSn platform, with a rocking curve FWHM of 0.18°.

4.3.2 GaAs/STO/Si. One further method worthy of note lies in growing a GaAs/Si HS through an intermediate $SrTiO_3$ (STO) layer. This method of GaAs growing was first announced in 2001 in Ref. [160], where a previously developed technique of epitaxially depositing STO on Si [161] was used to epitaxially grow GaAs onto this insulator [162, 163]. The growth of STO was initiated by jointly depositing Sr and Ti in the presence of oxygen at a substrate temperature of 200 – 400 °C [161, 164]. High consumers' properties of the resulting HSs were reported: no antiphase domains, a dislocation density in GaAs of about 10^5 cm^{-2}, and a surface root-mean-square roughness of about 0.9 nm. The electron mobility in GaAs/Si amounted to 94% of that in the reference GaAs/GaAs sample [163].

In Ref. [162], device quality GaAs/STO/Si heterostructures were reported to have been grown by MBE at Motorola laboratories on Si substrates 200 and 300 mm in diameter. FETs fabricated on these heterostructures showed quite encouraging characteristics: current channel degradation in a GaAs/STO/Si sample was 1.2% after 800 h of operation at 200 °C. The analysis of these studies led Chediak et al. [165] to the conclusion that the authors of works [162, 163] had been able to produce device quality GaAs-on-Si films.

However, the mechanisms responsible for the growth of perfect GaAs films in the GaAs/STO/Si configuration have not been established, nor did our database research reveal the continuation of the above studies or any investigations along the same lines by other authors. Furthermore, on 31 January 2003, a note was published on the site EETIMES, in the section 'Silicon Strategies', to the effect that Motorola Inc. had ceased the commercialization of this technology. As the note says, it remains unclear whether the reduced cost of GaAs substrates, the engineering problems of GaAs/STO/Si technology, or a combination of both were the reason for this.

5. GaP-on-Si epitaxy

5.1 Initial stages

The growth of GaAs on Si(001) substrates through a GaAsP (or InGaP) buffer layer with the variable composition is one of the little-studied approaches to obtaining a lattice constant transition from Si to GaAs. What makes this approach special is that at the initial — namely, GaP/Si — stage of the growth the lattice constant mismatch between these materials is rather small (∼ 0.37%). It was suggested that this should facilitate the epitaxial transition from Si to III – V compound-based solid solutions. A number of studies relevant to understanding GaP-on-Si(001) growth peculiarities should be mentioned [64, 130, 166 – 172].

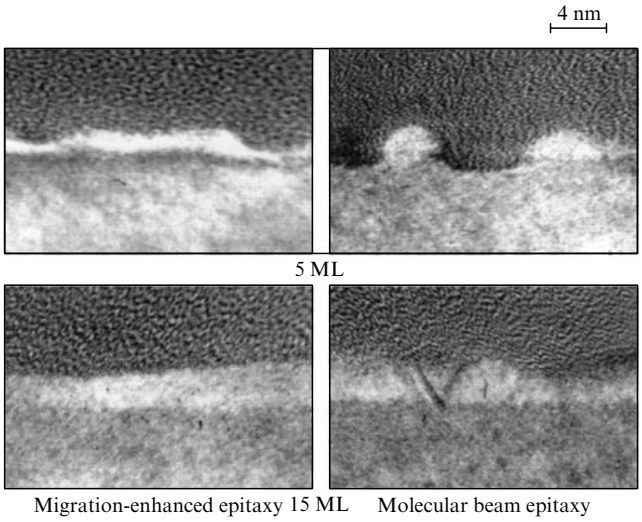

Figure 15. High-resolution electron microscope cross section images of GaP/Si(001). Film thicknesses are 5 and 15 ML. (Taken from Ref. [170].)

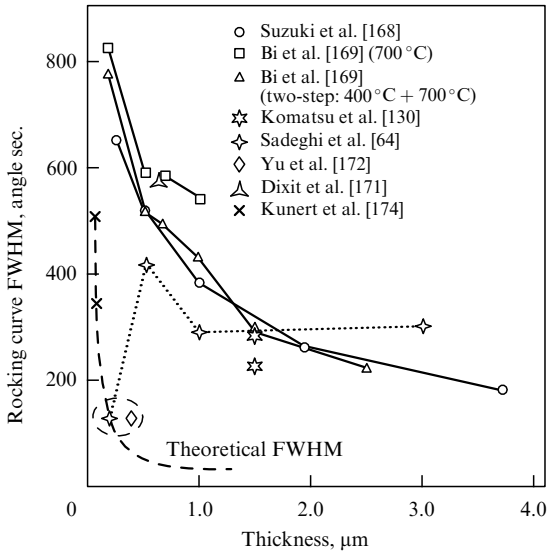

Figure 16. Full width at half maximum of the (004) X-ray rocking curve versus the thickness of a GaP film on an Si substrate as given by various authors.

Detailed studies of the initial stages of GaP-on-Si(001) growth using RHEED and high-resolution electron microscopy showed that, similar to GaAs/Si, the main problem here is to obtain a continuous perfect GaP layer because the nucleation occurs by the VW mechanism, i.e., the process involves the formation of separate large-sized islands whose coalescence gives rise to defects with high densities. Practically all researchers report that immediately after the epitaxial growth of GaP/Si starts, RHEED patterns show the formation of point reflections, pointing to the 3D character of the growth process. Takagi et al. [170] note that the phosphorous- stabilized Si(001) surface is chemically passive, and that the trend to the islanding growth of GaP is even observed if the migration-enhanced epitaxy of GaP is used at the initial stage. Figure 15 presents images (taken from Ref. [170]) of the cross sections of GaP/Si HSs at the initial stages of growth for different growth techniques. In the case of MBE, one observes pure islanding growth, whereas for migration-enhanced epitaxy only a trend to 3D growth is seen. Still, as the authors note, when the growth was done by alternating Ga and P layers, dislocations were introduced into the continuous layers, and at the stage of separate islands no dislocations were observed to be generated.

5.2 Comparison in terms of general structural perfection

Two-step growth [130, 167, 169], thermocycling [130], and migration-enhanced growth [64, 170, 173] led to a considerable improvement in the structural characteristics of GaP films grown on Si(001). The structural quality of a film can be estimated in general terms by measuring the full width at half maximum of the (004) X-ray rocking curve. Figure 16 demonstrates results from various studies on the GaP-film thickness dependence of this characteristic for the GaP/Si. The figure displays a large spread of data for film thicknesses up to 0.5 μm, confirming the key role of the initial stage of film formation. Despite the small Si–GaP lattice parameter mismatch, the formation of a continuous thin GaP layer on an Si surface practically never occurs, and it is for this reason that a large number of defects form at the very early stage of film formation and that, correspondingly, the X-ray rocking curve peak is considerably broadened. Shown in the same figure is the theoretical dependence of the rocking curve peak FWHM for perfect GaP films, allowing the crystal perfection of real films to be estimated. A noteworthy fact is the ultralow values of rocking curve FWHM cited in works by Sadeghi and Wang [64] and Yu et al. [172] for thicknesses of 0.2 and 0.4 μm, respectively. These values are circumscribed by a dashed oval in Fig. 16. For the left point [64], the film (of thickness 0.2 μm) can be thought of as pseudomorphic and defect-free — hence the small, near-theoretical rocking curve FWHM. As evidence that such films do exist, we used results from a talk by Kunert et al. [174], who claim to have grown the thinnest GaP-on-Si films ever reported to be studied by X-ray diffractometry.

Judging from the X-ray rocking curves presented in Ref. [174], the MOVPE-grown GaP films were pseudomorphic: the additional periodic peaks seen on the rocking curves were indicative of a high degree of parallelity between the film surface and the interface's reflection planes. (We used the peak-to-peak angular distance to estimate the thickness of the GaP films.) The rocking curve FWHM values for such films are given in Fig. 16. It is seen that these values practically fall on the theoretical dependence, thus indicating that the films are defect-free and thereby confirming that a continuous defect-free GaP layer can be grown as a pseudomorphic layer on Si(001). Yet, when the GaP film thickness exceeds a certain value, MDs are unavoidably introduced. As evidenced from Fig. 16, the rocking curve FWHM value for the higher-thickness (0.5 μm) GaP film from the study by Sadeghi and Wang [64] (the experimental points of these authors are dot-connected in the figure) is considerably higher, approaching what is found for most films of this thickness.

The right point in the dashed oval of Fig. 16 — the one for a film thickness of 0.4 μm — corresponds to the completely relaxed state, according to the authors of Ref. [172]. Such a film has to contain a certain number of TD type defects, and yet it has an FWHM of about 130″, which is the smallest value published for these GaP/Si thicknesses — the one close to the theoretical value. An analysis of the structural characteristics of the GaP/Si HSs is not sufficient alone to explain the difference from the data of other investigations.

However, the appearance of such the parameters should be taken into consideration.

6. GaAs growth on 'compliant' substrates

A 'compliant' (or 'soft') substrate is currently understood to mean an artificially created platform for epitaxial film growth, whose near-surface material (for example, porous silicon) possesses much lower elasticity constants compared with the material to be grown, or an ultrathin layer (membrane) which is located on a viscous substrate and gives orientation to epitaxial growth (see Fig. 17). In the latter case, such a buffer layer is silicon oxide (SiO_2) whose softening point is about 1200 °C, in particular, an artificial substrate of the silicon-on-insulator (SOI) type or borophosphatesilicate glass (BPSG) with a much lower softening point of about 500 °C. Moreover, the term compliant substrate also refers to structures created by directly joining dissimilar crystalline materials using the so-called twist-bonding technique [175]. The reader is referred to several review papers [176 – 181] for a detailed description of techniques for creating various versions of such platforms.

An early hypothesis was that, as a result of stress redistribution between the pseudomorphic epilayer and the thin membrane, the latter slides over its underlying viscous surface [182], so that the former, which elastically relaxes, remains structurally perfect and does not contain dislocations which are necessary for stressed layers to be able to plastically relax. Another often-suggested mechanism is the bending of a TD into the 'softer' substrate layer [183].

That relaxed films grown on compliant substrates are indeed characterized by a higher level of structural perfection has been shown in many studies whose results in this respect have been summarized in reviews [177 – 179]. However, more careful studies have largely ruled out the earlier suggestions that relaxation might occur through elastic deformation redistribution between the film and the thin membrane (or a lower elasticity region — porous silicon, for example). In fact, if the film being deposited starts growing as pseudomorphic and then elastically relaxes without forming TDs, then the deformation of the film is transferred to the compliant membrane. The ultimate lateral dimensions of the film — following the elastic relaxation — and the elastically extended membrane should exceed their initial values by the value of the lattice constant mismatch. Hence, for reasonable substrate dimensions, both the epitaxial film and the membrane should slide over the rigid substrate unhindered for large distances of fractions or even units of millimeters. The fact that this mechanism is quite unlikely to occur was brought to scientific attention by Kästner and Gösele [178] as early as 2000. Despite the huge amount of experimental data on the subject, and despite many published analyses of the data, the gliding of an extended relaxing film over a substrate has remained elusive. What has been discovered, though, is the buckling (or wrinkling) of an epitaxially grown stressed film.

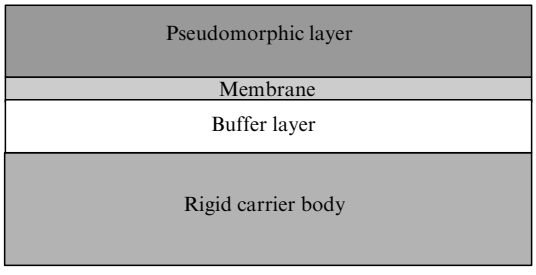

Figure 17. Schematics of epitaxial growth on a 'compliant' substrate comprising a viscous buffer layer of SiO_2 or borophosphatesilicate glass.

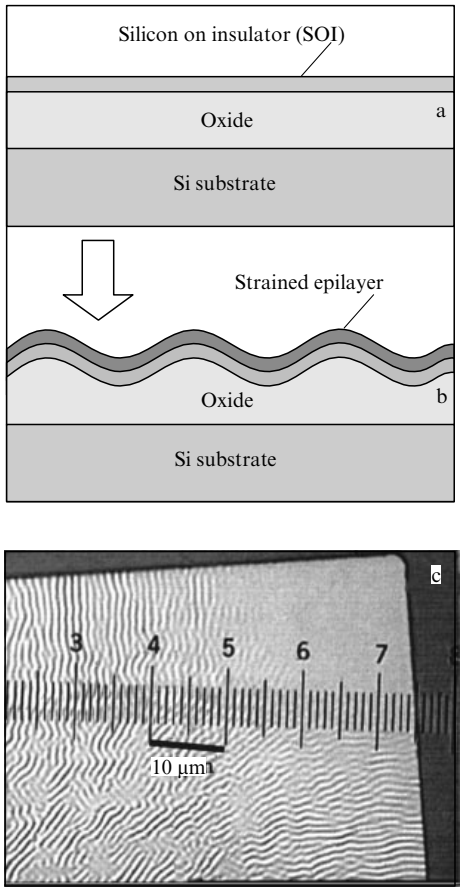

Figure 18. (a, b) Schematics of the way in which a stressed layer relaxes elastically via the formation of wrinkles or buckles; (c) elastic relaxation of a GeSi mesoisland on a viscous buffer layer via the buckling of its central part. (Courtesy of the authors of Ref. [185].)

The interface between the membrane and the substrate usually contains various types of defects (steps, inclusions, impurities, etc.) which prevent the membrane from freely gliding large distances and which make this impossible for it without the elastic relaxation of the film due to its bending. The same problem remains for the plastically relaxing membrane if the introduction and gliding processes and those of interaction between dislocation semiloops are localized in the compliant layer. The gliding process of the layer – membrane heteropair over the rigid substrate should start spontaneously at various points randomly distributed over the substrate surface — unavoidably causing individual regions to glide opposite to one another and leading to the formation of a cellular structure. This effect, namely, the formation of wrinkles on a layer residing on a viscous base, has been the subject of considerable study [184 – 186]. Figures 18a, b are schematics of how a film surface becomes wrinkled. The growing stressed epilayer relaxes elastically due to increasing lateral dimensions but, instead of gliding along the soft buffer layer together with the stretched membrane, it acquires a characteristic wrinkled surface due

to the periodically changing buffer layer thickness. However, if the temperature is not high enough for the buffer layer to manifest its viscous properties, the stressed layer relaxes as usual through the introduction of TDs. Rehder et al. [187] compared the dislocation structures of relaxed GeSi films grown on bulk Si and SOI substrates. In the latter case, the thickness of the silicon membrane ranged from 40 nm to 10 μm. The authors note that in all the cases studied the film relaxation mechanism was via the introduction of TDs and that the relaxation process was independent of the substrate type used.

As shown in Refs [185, 188], it is only if a stressed film residing on a viscous buffer layer is laterally small that it relaxes by elastically stretching itself due to its gliding over such a layer. Yin et al. [185], who studied the relaxation of pseudomorphic, 30-nm-thick $Ge_{0.3}Si_{0.7}$ islands bonded to the Si substrate via a layer of borophosphatesilicate glass, observed that, when annealed, mesoislands relax elastically — primarily due to buckling (Fig. 18c). It is only at the corners of the islands, within 10 to 20 μm, that gliding of the film along the interface as a relaxation mechanism for elastic deformations is seen to prevail over the buckling. This is clearly seen in the photo in Fig. 18c of the surface near such a mesoisland corner.

Tezuka et al. [188] showed that GeSi-on-SOI mesoislands 5 μm or less in diameter fully relax without forming TDs, when annealed at 1000 – 1200 °C. This is evidenced by the fact that the surface of these islands does not contain the characteristic cross-hatches that mark places where gliding dislocations emerge on the surface. Such cross-hatches were, however, present on the extended (more than 300 μm) sections of the GeSi film, which were located on the same substrates.

All of this being so, why then does the compliant substrate improve the structural characteristics of the extended layer being grown and, in particular, why does the TD density decrease? As is known, if a stressed film relaxes by the introduction of TDs, then what determines the relaxation rate is the number — and mobility — of the tilted branches of 60° MDs (see, for example, Ref. [180]). For a reduced TD density, the only way to achieve an acceptable plastic relaxation rate is by increasing their gliding velocity.

According to classical ideas [189] as adapted to a TD gliding in a stressed film [190], the velocity of a dislocation can be written in the form

$$V_{\mathrm{d}} = V_0(\tau_{\mathrm{eff}})^m \exp\left(-\frac{E_v}{kT}\right), \tag{3}$$

where V_0 is a constant, E_v is the dislocation gliding activation energy, the number m ranges between 1 and 2 according to various data (see, for example, Ref. [191]), and τ_{eff} is the effective shear stress [192] determining MD nucleation and TD propagation process in a stressed film. For a film of thickness h, one obtains

$$\tau_{\mathrm{eff}} = S\,\frac{2G(1+\nu)}{1-\nu}\,\varepsilon - \frac{Gb(1-\nu\cos^2\alpha)\cos\phi}{4\pi h(1-\nu)}\left(\ln\frac{\beta h}{b}+1\right). \tag{4}$$

The first term in Eqn (4), $\left[2G(1+\nu)/(1-\nu)\right]\varepsilon$, represents the biaxial stress in the film and is the driving force of the plastic relaxation process. Here, G and ν are the shear modulus and Poisson's ratio, respectively. The effect of the stress component along the TD motion is accounted for by the quantity $S = \cos\lambda\cos\phi$, the so-called Schmidt factor, where ϕ is the angle between the gliding plane and the interface normal, and λ is the angle the dislocation Burgers vector **b** makes with the perpendicular (lying in the interface plane) to the intersection of the dislocation gliding and interface planes. The second term on the right-hand side of Eqn (4), the shear stress component hindering TD motion, is calculated from the work needed to produce a new MD of unit length. In Eqn (4), α is the angle between the dislocation's line and Burgers vector. The number β, known as the dislocation core parameter, is, in accordance with current data for GeSi, taken to be 0.76 (for 60° dislocations) [193]. As seen from Eqn (3), the threading dislocation gliding velocity at a constant temperature can be increased by increasing the effective shear stress τ_{eff} and/or by decreasing the activation energy E_v. Given this, a discussion of plastic relaxation mechanisms in films grown on compliant substrates is in order.

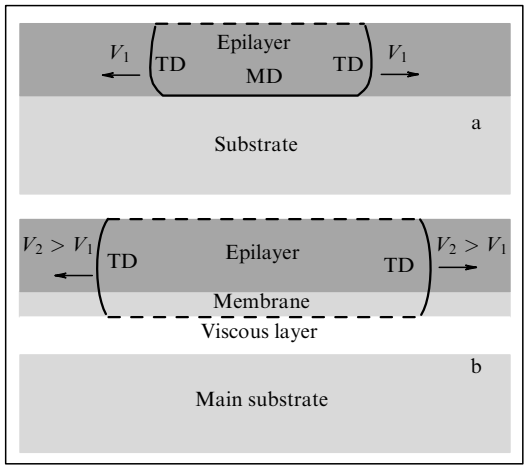

Figure 19. 'Disappearance' of a misfit dislocation in a heterostructure grown on a substrate-membrane located on an amorphous buffer layer. (Taken from Ref. [178].)

Kästner and Gösele [178] contributed most heavily to the revision of the relaxation mechanisms for such films. Returning to the plastic relaxation of deformations as an alternative to their elastic relaxation, Kästner and Gösele suggest a modification to this concept. Figure 19a presents a standard scenario for MD formation at the stressed film – substrate interface. In the presence of an amorphous or amorphousized buffer layer near the interface, the MD 'drowns' in this buffer layer (Fig. 19b), being drawn from the film – membrane interface by forces similar to image forces acting on the dislocation line near the film surface. Exactly as in the case of a free surface, a dislocation leaves a step at the membrane–viscous layer interface (as shown dashed in Fig. 19). The additional energy due to the appearance of such a step is, as in the free surface case, much less than the MD energy at the interface. It is this difference which makes an MD move to the membrane – 'lubricating' layer interface. The MD formation work becomes correspondingly smaller.

Because the decelerating forces preventing the TDs from running apart decrease [see Eqn (4)], the critical thickness for the introduction of MDs decreases, rather than increases as it should be according to calculations assuming elastic deformation redistribution between the film and the compliant

membrane. This causes the MDs to move faster, thus lowering their final density. A similar situation is possible if porous silicon or a system of screw dislocations following twist-bonding are used as a 'lubricating' layer.

The possibility of influencing the value of the activation energy E_v may provide another explanation for the improved structural characteristics of plastically relaxed films grown on compliant substrates. As is known, the commonly accepted dislocation motion model is that involving the formation of the double [194] and single [195] dislocation kinks. Because of thermal fluctuations and the action of stresses, a double kink can start on a dislocation line. After the critical size is reached, the double kink dissociates into two single ones that run apart in opposite directions, resulting in the dislocation line moving to the neighboring valley of the energy relief. Thus, the gliding velocity of a dislocation is controlled by the kink formation energy F_k and the height W_m of an energy barrier for kink migration. According to Refs [194, 196], the dislocation motion activation energy in Eqn (3) consists of two parts: $E_v = 2F_k + W_m$, the activation energy for the formation of a double kink, and the activation energy for kink migration. It is hypothesized that this mechanism for the formation of a double step shows up in bulk samples and buried films [197].

Hull et al. [198] provided theoretical and experimental evidence that the formation of a single kink near the free surface of a stressed film is more favorable energetically and leads to a severalfold increase in the TD propagation velocity compared with buried GeSi films. In the compliant substrate case, the membrane – viscous layer interface can be thought of as an additional free surface that produces single kinks on the dislocation line, thus decreasing E_v and speeding up TD gliding. It is in this way that Ref. [187] explains how a compliant substrate improves the structural properties of films.

As seen from the above, the effect of substrate compliance on the structural properties of films was mainly studied in the GeSi/Si system — both because these HSs are being widely grown and because they allow a smooth 0 – 4% lattice mismatch variation between the film and the substrate. Growing GaAs/Si using the possible advantages of a compliant-effect substrate has been given only limited study. Seaford et al. [199] used SOI(511) substrates (which they called compliant) to grow GaAs/Si films. Because the Si membrane was taken to be 100 nm thick and the GaAs growth temperature to be about 580 °C (the latter ruling out the viscous softening of the oxide), the SOI substrate was unlikely to exhibit compliance mechanisms. Yet, the authors claim that the rocking curve FWHM of their 4-μm-thick GaAs film was 25% less than for GaAs growth on a bulk Si substrate having the same (511) orientation. As seen in Fig. 6, where this FWHM is shown, its value (150″) considerably exceeds those from other researchers, who grew GaAs films without using the compliance effects.

Pei et al. [200] also grew GaAs on SOI(511) with Si membranes with thicknesses of 100 and 200 nm. They achieved an X-ray rocking curve FWHM of 128″ for gallium arsenide films 3 μm thick grown on such substrates. As seen in Fig. 6, this value falls within the range of minimum FWHM values for this particular thickness of GaAs/Si, but does not differ from them significantly. In the authors' proposed scenario, MDs are drawn from the stressed film – Si membrane interface to the Si membrane – SiO_2 interface, thus expectedly increasing the gliding velocity and decreasing the number of MDs. However, as analysis of the early nucleation and growth stages of GaAs on Si shows (see Section 3), the main structural defects develop in this system when the nucleation and coalescence of GaAs islands occur — the time when the average thickness of the GaAs film is several monolayers, much less than the thickness of the Si membrane. The membrane in this case serves as a bulk substrate, and effects hypothesized to be due to its compliance should be absent.

Thus, the scarce experimental data available on the growth of GaAs films on Si (SOI) substrates provide no evidence for the considerable improvement in the structural characteristics of GaAs/Si heterostructures, nor is research along these lines attractive enough economically to encourage hopes for further work.

7. Nonepitaxial GaAs – Si techniques (bonding)

The generic term 'wafer bonding' refers to attaching bulk or thin-film GaAs (as well as other semiconducting III – V compounds) to various, primarily Si, substrates. One solid can be joined directly to another at a temperature as low as room temperature by pressing together mirror-polished, flat, ideally clean surfaces. When joined in this way, the surfaces start interacting with each other at the atomic level by means of van der Waals forces. The reader is referred to Gösele et al. [201] for an in-depth historical review of research into this technique. The direct joining of two surfaces requires that they be thoroughly processed, including planarization, roughness minimization, and careful removal of surface contamination [202 – 204]. In another approach, one solid is 'glued' to the other at a high temperature by first coating the two surfaces with glassy films and then pressing the surfaces together at the films' softening temperature. This bonding is often referred to as wafer bonding. In the work by Antypas and Edgecumbe [205], who were the first to use this wafer bonding in semiconductor technology, the GaAs/AlGaAs heterostructure was bonded to a glass substrate to fabricate GaAs-based transmission photocathode. The GaAs substrate was removed, and the thick glass was used as a transparent carrier substrate for the AlGaAs/GaAs/AlGaAs HS that remained on the glass.

Figure 20 is a schematic of the process currently used to transfer a GaAs film or a more complex HS — for example, a laser structure — onto a bulk Si substrate. A point of principle in this technological diagram of the bonding process is to develop a technique for selectively etching off the GaAs substrate. For this purpose, the epitaxial deposition of a GaAs layer or a complex HS containing several dissimilar layers is preceded by growing onto a GaAs substrate a so-called stop layer with the function to stop the etching of the GaAs substrate. For a GaAs/AlGaAs-based system of layers, AlGaAs with a high content of Al serves as a stop layer. The completed heterostructure and the Si substrate are coated with a layer of oxide (Fig. 20a, b) and joined at a certain pressure at the oxide's softening temperature (Fig. 20c). First the GaAs substrate (Fig. 20d) and then the stop layer are etched off, leading, at the oval-dashed position in Fig. 20e, to a new artificial substrate, or platform, on which the existing GaAs layer either is thinned out and smoothed out by chemical – mechanical polishing to the desired thickness and desired surface smoothness (Fig. $20f_1$), or, as another possibility, the epitaxial growth of a new GaAs layer takes place (Fig. $20f_2$). With this organization of the artificial GaAs/Si substrate, each particular implementation involves

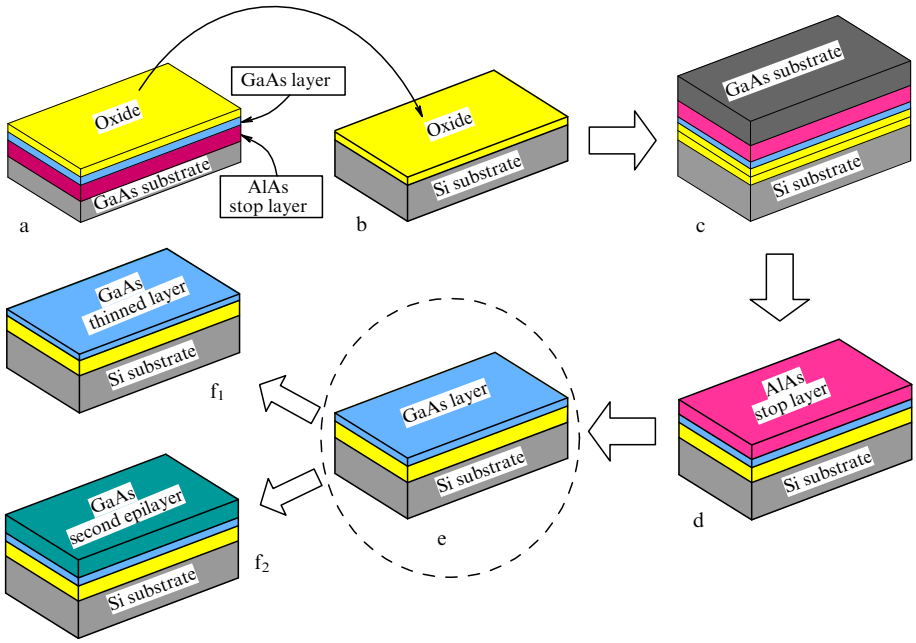

Figure 20. Schematic of fabricating an artificial GaAs/Si substrate by the wafer bonding method.

the destruction, via etching, of the primary GaAs substrate used for growing the transferable HS, which considerably complicates the technology and makes it much more costly. Still, nonepitaxial bonding techniques add another degree of freedom to the field, allowing production of material combinations unachievable by epitaxial growth.

At present a range of media containing dissimilar materials have been developed: SiO_2-SiO_2 (deposition of SiO_2 on the surfaces of both the materials being bonded) [206, 207]; borophosphatesilicate glass deposited in a variety of ways, including that from the liquid phase [208, 209]; SeS_2-SeS_2 [38], and a thin viscous coating is deposited onto both wafers being bonded by centrifuging from solutions based on silane (Si–OH) and methyl (CH_3) polymers dissolved in an alcohol–acetone mixture [210, 211]. The fundamentals of the technology of bonding semiconductor materials can be found discussed in a review by Gösele and Tong [212]. As noted in Section 2, transferring a GaAs epifilm to an Si substrate using a nonepitaxial bonding technique can be performed without noticeably compromising the structural characteristics of the film. The record-low rocking curve FWHM of 44″ measured for such a GaAs film of 3 μm thickness grown on an Si substrate [38] (see Fig. 6) supports this conclusion.

8. GaAs/Si-based devices

In spite of over twenty years of research, GaAs/Si HS devices are still at the pilot sample development stage. As noted earlier in the paper, the benefits of integrating optoelectronic GaAs-on-Si devices are the following: GaAs substrates can be replaced by lower-cost, higher-strength, higher-thermal-conductivity Si substrates in developing high-power amplifiers with parameters superior to those of Si transistors; the GaAs/Si system can be used as a platform for developing solar cells, injection heterolasers, photodetectors, waveguides, and modulators, and GaAs optoelectronics and traditional silicon ICs can be combined on one plate. In the first two cases, the GaAs/Si system is used as a new carrier, and the various techniques for fabricating this platform that are described in preceding sections (including high-temperature annealing and thermocycling processes) have led to quite positive results [161–163, 213–230].

The defects that deteriorate the parameters of GaAs/Si devices most are threading dislocations (which is the reason why the preceding sections mainly concentrated on how to lower their density). For transistors operating on majority carriers, a high dislocation density manifests itself in reduced electron (or hole) mobility, whereas minority-carrier devices (solar cells, light diodes, and injection lasers) are more sensitive to these defects. Dislocation density in such structures should be less than 10^6 cm^{-2}. As already noted in Section 3.3.2, Motorola-produced FETs based on GaAs/STO/Si HSs MBE-grown on Si substrates 200 and 300 mm in diameter have very similar properties to reference GaAs/GaAs samples [161–163].

After many years of development work on the growth technology of the Ge/GeSi/Si type HSs, an MIT team led by E Fitzgerald created a platform with which most GaAs technology-based devices can be fabricated, with comparable parameters to analogous devices on GaAs and Ge substrates. To date, due to the graded buffer layer of GeSi alone, the dislocation density in the operating region of a GaAs film can be stably lowered to below 10^6 cm^{-2} — with the result that the minority-carrier lifetime in GaAs/Si have exceeded 10 ns [122]. Such high structural parameters of the platform with a graded lattice constant transition from Si to GaAs have allowed a number of minority-carrier devices to be developed [106, 217, 218, 231]. In 2007, the MIT team went a step further by using the Ge/GeSi/Si platform to fabricate AlGaAs/GaAs-based heterojunction bipolar transistors [229].

Whereas GaAs-based solar cells used with light concentrators and in space normally use Ge as a substrate, the Si substrate offers significant advantages over its Ge counterpart, due to lower specific weight, higher mechanical strength and thermal conductivity, lower cost, and larger-sized plates (i.e., silicon substrates). Therefore, the focus of many

researchers has been on developing Si-based photovoltaic platforms and studying the basic characteristics of such solar cells [213 – 221].

The one-plate integration of GaAs optoelectronics and traditional silicon ICs is still at the research stage. The fact that the GaAs and Si surfaces are far apart in thickness — the separation distance exceeds 10 μm in the case of graded buffer layers of Ge/GeSi/Si — presents an insurmountable obstacle to using high-resolution photolithography and arranging Si-III – V connections on the same plate. Furthermore, the annealing and thermal cycling of GaAs/Si HSs — high-temperature treatments which considerably improve the crystal perfection of these platforms — are unsuitable for growing GaAs in the windows of Si substrates with off-the-shelf IC elements. With this recognition, the authors of Refs [227, 232] propose a new — Si/Ge/GeSi/Si — platform. They use the method of wafer bonding via thin oxide films (see Section 7) to bond a thin Si layer to the Ge/GeSi/Si HS, resulting in a distance (in thickness) of less than 1 μm between the upper Si layer and its Ge undercoating [232]. In the windows etched off in the upper Si layer and in the oxide (i.e., on the Ge surface), high-quality III – V heterostructures can be grown. Reference [227] demonstrated the operation of a matrix of AlGaInP heterostructure LEDs grown in the windows of such a platform. Such artificial substrates, the authors believe, provide one possible way to realize ICs in silicon with optical bonds.

In the approach proposed by Oye et al. [230], it is assumed that realizing an IC combining silicon and GaAs elements primarily requires GaAs films with ultralow surface roughness on thin buffer layers — without intermediate chemical – mechanical polishing and without high-temperature annealing. The work suggests special conditions for growing GaAs films on silicon. First, MBE was applied to deposit on an Si substrate graded GeSi layers of stepwise-variable composition, whose major feature is small thickness (their total thickness is 80 nm). This is followed by growing GaAs using the MEE technique. The root-mean-square surface roughness of such platforms was less than 1 nm; on such substrates, III – V-based capacitors (MOSCAPs) have been fabricated. Notice, however, that the structural characteristics, in particular, the dislocation density, of the GaAs-based films used are not specified in this work.

9. Conclusions

For over twenty years researchers have attempted to combine Si and GaAs on the highest-efficiency silicon substrate. Alternative GaAs-on-Si substrates have a considerable market potential for replacing the costly GaAs substrate in producing traditional GaAs devices such as solar cells, photodetectors, LEDS, lasers, and microwave devices, and as a new technology for monolithic integration of GaAs elements and silicon integrated circuits. An additional factor that enhances the prospects for GaAs-on-Si technology is the miniaturization of silicon integrated circuits and their corresponding approach to the physical limit in terms of size. It is becoming possible to make integrated circuits to operate faster without reducing the size of their elements through the fiber-optic integration of GaAs-based lasers and photodiodes with silicon signal processing circuitry. However, despite some emerging successes in developing perfect GaAs/Si HSs and despite the realization of some applications, no significant progress can be claimed in this field.

By the last decade of the twentieth century, the basic problems encountered in growing GaAs on Si were identified and documented. The most noteworthy of these is the growth of a polar semiconductor on a nonpolar substrate, leading to a large density of antiphase domains. This problem was successfully solved by using Si substrates deflected through $4^\circ - 6^\circ$ from the singular (001) plane. Other problems turned out to be more serious. Due to the approximately 4% film – substrate lattice mismatch in the GaAs/Si system, the dislocation density in the GaAs films reaches values of $10^9 - 10^{10}$ cm^{-2}. The difference in thermal expansion coefficients also favors the copious dislocation formation in and the cracking of a GaAs film as the film is cooled. These problems still remain and are being solved with mixed success using a variety of techniques, including the two-step growth of GaAs, the thermocycling of an as-grown HS, and growing buffer layers of other materials. As of today, with the technique of graded buffer layers of GeSi alone it has proved possible to obtain GaAs films with a dislocation density of 10^6 cm^{-2} and less in the operating region, resulting in minority-carrier lifetime of more than 10 ns in GaAs/Si. Such high structural properties of the platform with graded lattice constant transition from Si to GaAs have enabled a range of minority-carrier devices to be developed (including solar cells, LEDs, and injection lasers), whose parameters are similar to those of devices based on homoepitaxial GaAs/GaAs structures.

The one-plate integration of GaAs optoelectronics and traditional silicon ICs is still at the research stage. The large separation (along the vertical) between GaAs and Si surfaces — exceeding 10 μm in the case of graded buffer layers of Ge/GeSi/Si — presents an insurmountable obstacle to carrying out high-resolution photolithography and arranging Si-III – V connections on the same plate. Moreover, various high-temperature treatments of the GaAs/Si HSs that considerably enhance the crystal perfection of these platforms — such as annealing and thermal cycling — are unacceptable for growing GaAs in the windows of Si substrates with off-the-shelf IC elements. For such integration to be possible, epitaxial GaAs heterostructures on Si(001) substrates need to be large in diameter, to have a GaAs film no more than 0.1 μm thick, and to have a near-surface dislocation density of no more than 10^6 cm^{-2} — requirements that are currently beyond possible reach and to whose solution no approaches can apparently be found in the literature reviewed here.

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